

Model Name : GA-G41M-Combo**Revision 1.3****SHEET****TITLE**

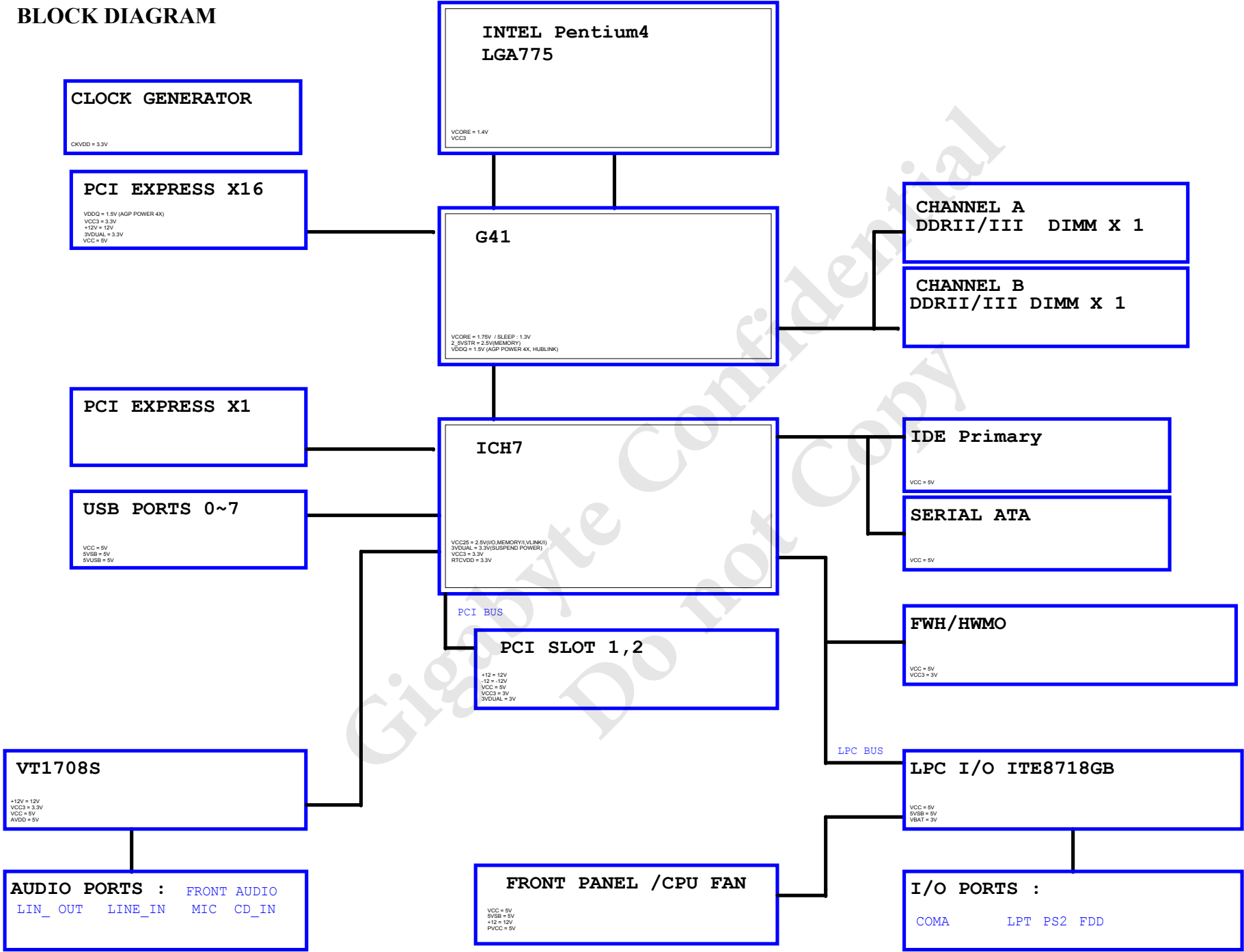
01	COVER SHEET
02	BLOCK DIAGRAM
03	BOM & PCB MODIFY HISTORY
04	P4 LGA775 A
05	P4 LGA775 B,D
06	P4 LGA775 C
07	P4 LGA775 E,F,G,H
08	G41 HOST
09	G41 DDRII/DDRIII
10	G41 PCI E, DMI
11	G41 VGA
12	G41 GND
13	G41 PWR
14	PCI EXPRESS*16 SLOT
15	DDR2/3 CHANNEL A
16	DDR2/3 CHANNEL B
17	DDR2/3 TERMINATION
18	ICH7 PCI, USB, DMI, LAN
19	ICH7 IDE, GPIO, SATA, CTRL
20	ICH7 VCC, GND
21	CK505 CLOCK.
22	PCI SLOT 1,2,PCIE*1
23	IDE/FLOPPY
24	ITE 8718 GB
25	COM LPT
26	CI,HWM,KB/MS,DUALBIOS
27	VT1708S

SHEET**TITLE**

28	REAR AUDIO JACK
29	DISCRETE POWER
30	VCORE PWM ISL6312
31	ATX, OTHERS POWER
32	FRONT PANEL
33	ATHEROS AR8151/8152

Gigabyte Technology			
Title			
Cover Sheet			
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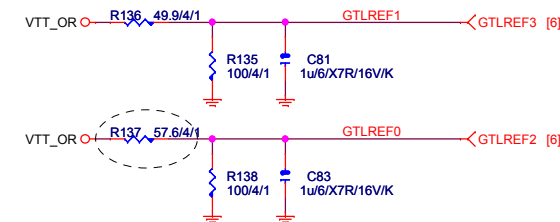
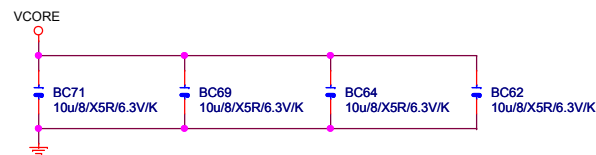
BLOCK DIAGRAM



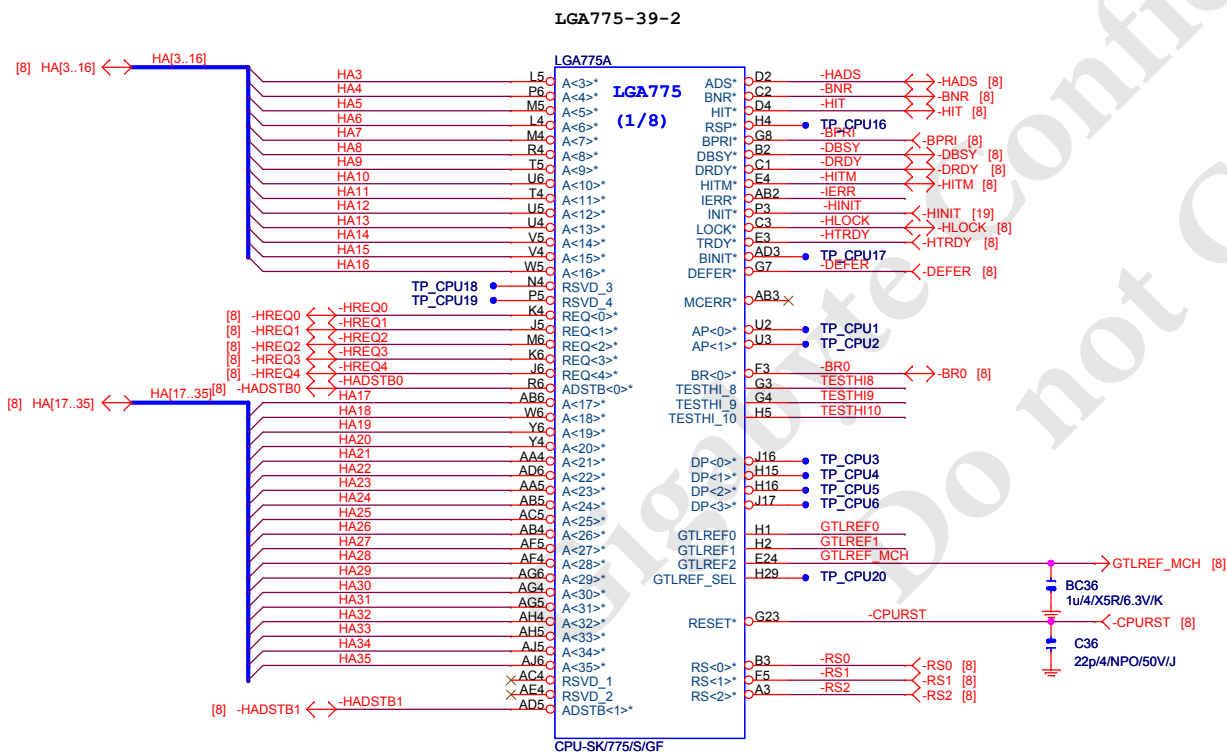
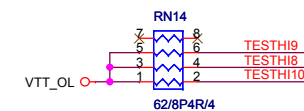
Version: 1.3

2010/05/11

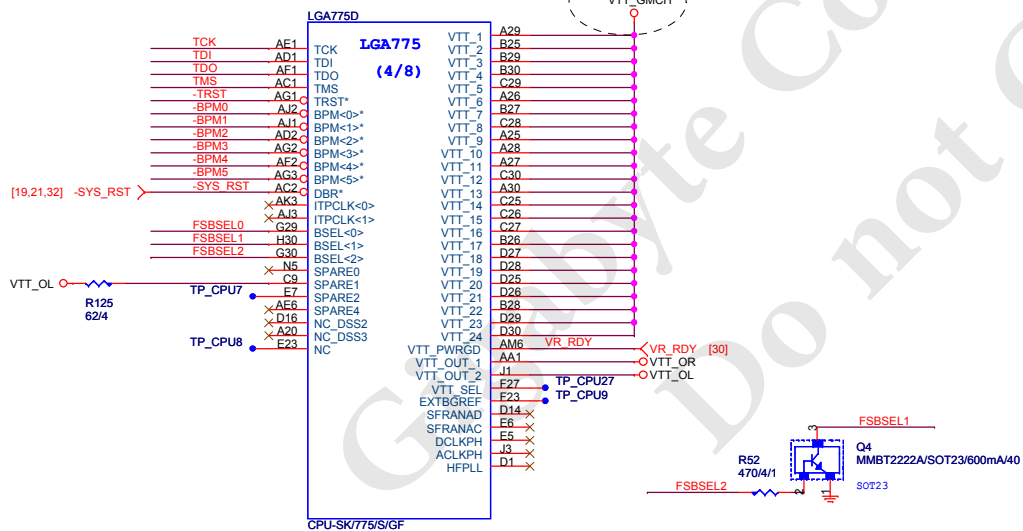
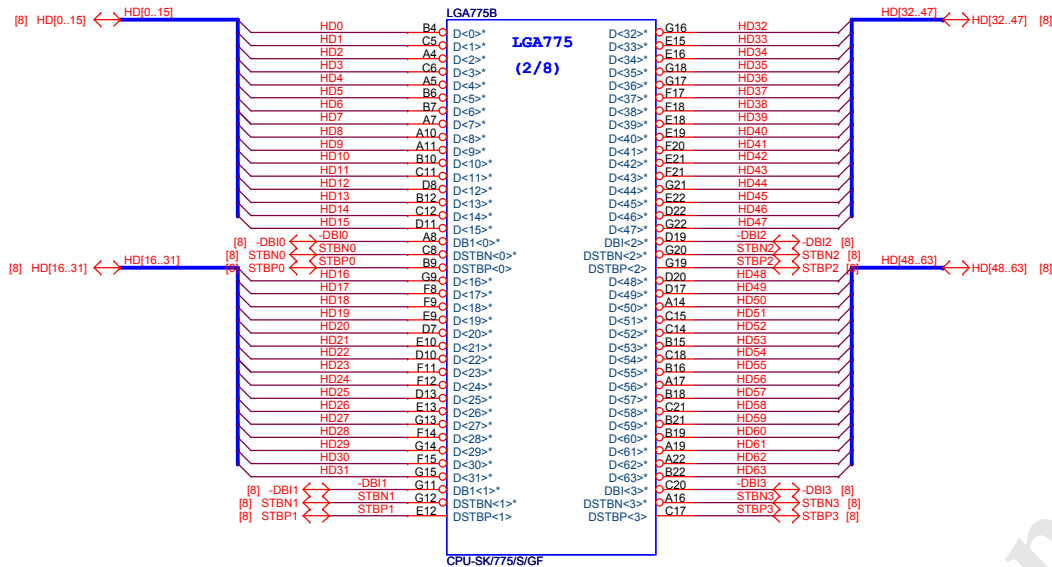
[illegible][illegible]



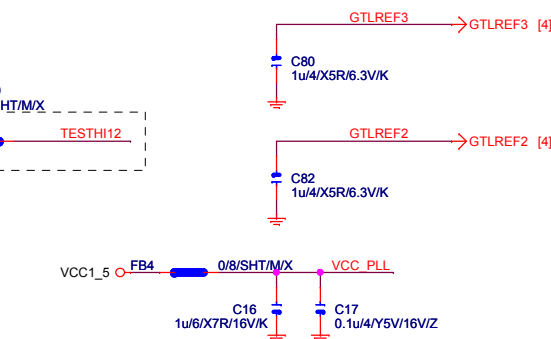
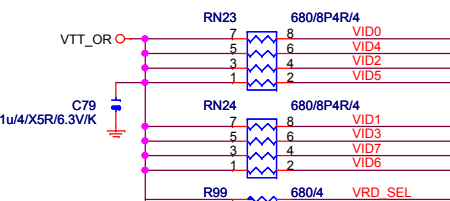
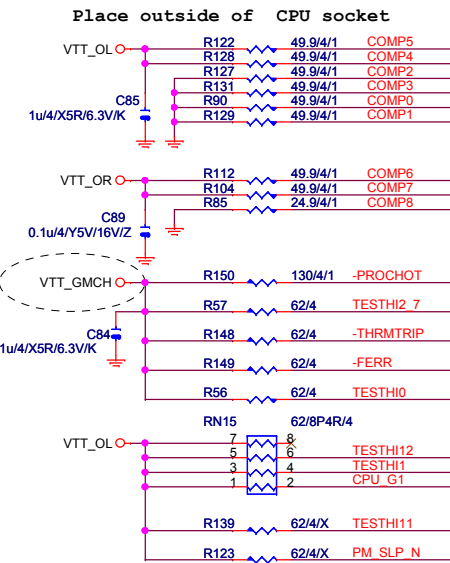
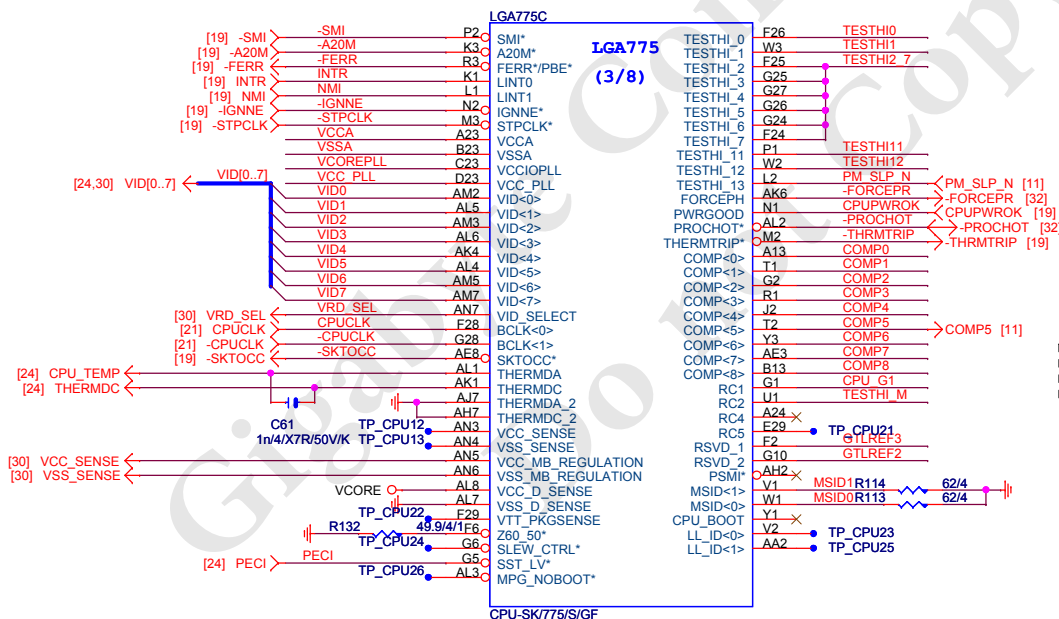
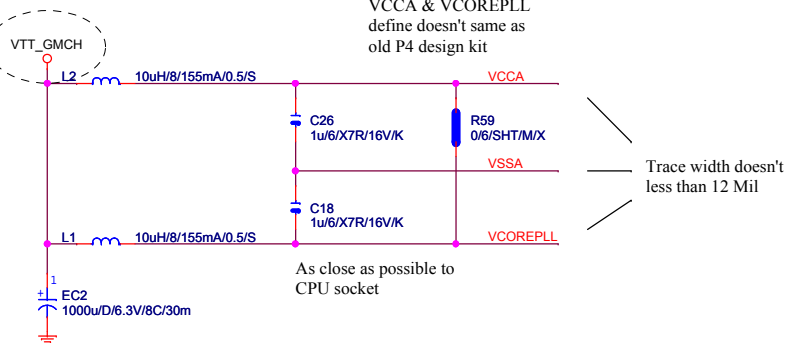
中間値0.9V



<p align="center"><i>Gigabyte Technology</i></p>			
<p align="center">P4_LGA775-A</p>			
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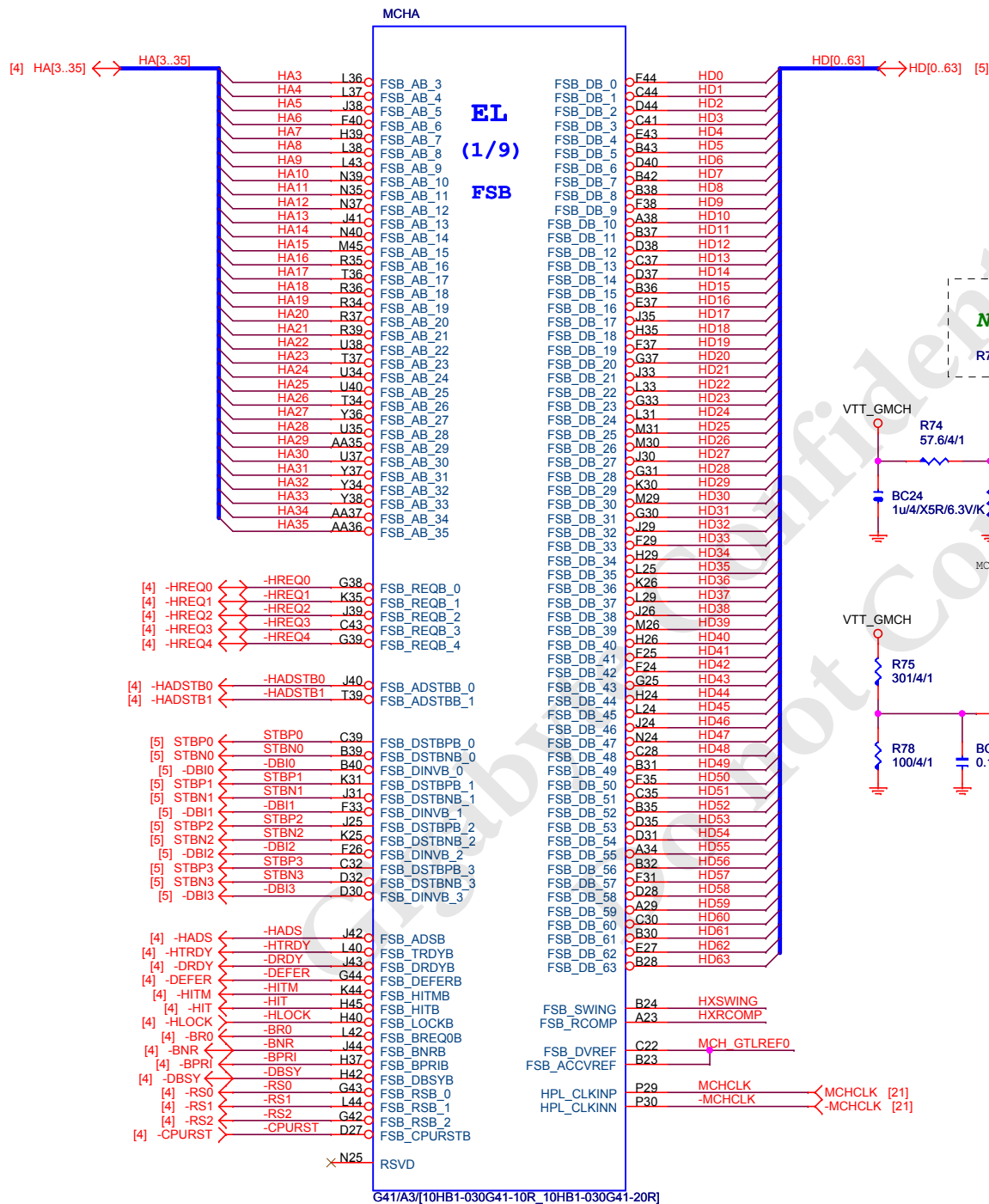
Note:
VCCA & VCOREPLL
define doesn't same as
old P4 design kit



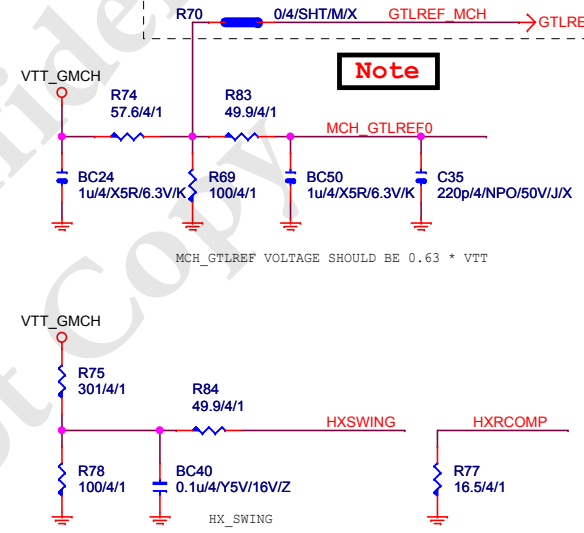
Gigabyte Technology			
Title			
P4_LGA775-C			
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PECI:Platform Environment Control Interface





Not used for CoreTM2 Duo and Wolfdale



Note

MCH_GTLREF VOLTAGE SHOULD BE 0.63 * VTT

MCHB

EXP_A_RXP0 F6
EXP_A_RXN0 G7
EXP_A_RXP1 H6
EXP_A_RXN1 G4
EXP_A_RXP2 J6
EXP_A_RXN2 J7
EXP_A_RXP3 L6

PEG_RXP_0
PEG_RXN_0
PEG_RXP_1
PEG_RXN_1
PEG_RXP_2
PEG_RXN_2
PEG_RXP_3(HB_HPD)

HDMI
/DVI
(B)

(HBTX2)PEG_TXP_0
(HBTX2#)PEG_TXN_0
(HBTX1)PEG_TXP_1
(HBTX1#)PEG_TXN_1
(HBTX0)PEG_TXP_2
(HBTX0#)PEG_TXN_2
(HBTXC)PEG_TXP_3
(HBTXC#)PEG_TXN_3

C11 EXP_A_TXP0
B11 EXP_A_TXN0
A10 EXP_A_TXP1
B9 EXP_A_TXN1
C9 EXP_A_TXP2
D8 EXP_A_TXN2
B8 EXP_A_TXP3
C7 EXP_A_TXN3

EXP_A_TXP[0..15] >>> EXP_A_TXP[0..15] [14]
EXP_A_TXN[0..15] >>> EXP_A_TXN[0..15] [14]
EXP_A_RXP[0..15] >>> EXP_A_RXP[0..15] [14]
EXP_A_RXN[0..15] >>> EXP_A_RXN[0..15] [14]

EXP_A_RXN3 L7
EXP_A_RXP4 N9
EXP_A_RXN4 N10
EXP_A_RXP5 N7
EXP_A_RXN5 N6
EXP_A_RXP6 R7
EXP_A_RXN6 R6
EXP_A_RXP7 R9

PEG_RXN_3
PEG_RXP_4
PEG_RXN_4
PEG_RXP_5
PEG_RXN_5
PEG_RXP_6
PEG_RXN_6
PEG_RXP_7(HC_HPD)

HDMI
/DVI
(C)

(HCTX2)PEG_TXP_4
(HCTX2#)PEG_TXN_4
(HCTX1)PEG_TXP_5
(HCTX1#)PEG_TXN_5
(HCTX0)PEG_TXP_6
(HCTX0#)PEG_TXN_6
(HCTXC)PEG_TXP_7
(HCTXC#)PEG_TXN_7

B7 EXP_A_TXP4
B6 EXP_A_TXN4
B3 EXP_A_TXP5
B4 EXP_A_TXN5
D2 EXP_A_TXP6
C2 EXP_A_TXN6
H2 EXP_A_TXP7
G2 EXP_A_TXN7

EXP_A_RXN7 R10
EXP_A_RXP8 U10
EXP_A_RXN8 U9
EXP_A_RXP9 U6
EXP_A_RXN9 U7
EXP_A_RXP10 AA9
EXP_A_RXN10 AA10
EXP_A_RXP11 R4
EXP_A_RXN11 P4
EXP_A_RXP12 AA7
EXP_A_RXN12 AA6
EXP_A_RXP13 AB10
EXP_A_RXN13 AB9
EXP_A_RXP14 AB3
EXP_A_RXN14 AA2
EXP_A_RXP15 AD10
EXP_A_RXN15 AD11

PEG_RXN_7
PEG_RXP_8
PEG_RXN_8
PEG_RXP_9
PEG_RXN_9
PEG_RXP_10
PEG_RXN_10
PEG_RXP_11
PEG_RXN_11
PEG_RXP_12
PEG_RXN_12
PEG_RXP_13
PEG_RXN_13
PEG_RXP_14
PEG_RXN_14
PEG_RXP_15
PEG_RXN_15

EL
(2/9)

PCIE

PEG_TXP_8
PEG_TXN_8
PEG_TXP_9
PEG_TXN_9
PEG_TXP_10
PEG_TXN_10
PEG_TXP_11
PEG_TXN_11
PEG_TXP_12
PEG_TXN_12
PEG_TXP_13
PEG_TXN_13
PEG_TXP_14
PEG_TXN_14
PEG_TXP_15
PEG_TXN_15

J2 EXP_A_TXP8
K2 EXP_A_TXN8
K1 EXP_A_TXP9
L2 EXP_A_TXN9
P2 EXP_A_TXP10
M2 EXP_A_TXN10
T2 EXP_A_TXP11
R1 EXP_A_TXN11
U2 EXP_A_TXP12
V2 EXP_A_TXN12
W4 EXP_A_TXP13
V3 EXP_A_TXN13
AA4 EXP_A_TXP14
Y4 EXP_A_TXN14
AC1 EXP_A_TXP15
AB2 EXP_A_TXN15

Close to MCH

[18] DMI_MCH_IT_MR_0_DP <> DMI_MCH_IT_MR_0_DP AD7
[18] DMI_MCH_IT_MR_0_DN <> DMI_MCH_IT_MR_0_DN AD8
[18] DMI_MCH_IT_MR_1_DP <> DMI_MCH_IT_MR_1_DP AE9
[18] DMI_MCH_IT_MR_1_DN <> DMI_MCH_IT_MR_1_DN AE10
[18] DMI_MCH_IT_MR_2_DP <> DMI_MCH_IT_MR_2_DP AE6
[18] DMI_MCH_IT_MR_2_DN <> DMI_MCH_IT_MR_2_DN AE7
[18] DMI_MCH_IT_MR_3_DP <> DMI_MCH_IT_MR_3_DP AF9
[18] DMI_MCH_IT_MR_3_DN <> DMI_MCH_IT_MR_3_DN AF8

DMI_RXP_0
DMI_RXN_0
DMI_RXP_1
DMI_RXN_1
DMI_RXP_2
DMI_RXN_2
DMI_RXP_3
DMI_RXN_3

DMI

DMI_TXP_0
DMI_TXN_0
DMI_TXP_1
DMI_TXN_1
DMI_TXP_2
DMI_TXN_2
DMI_TXP_3
DMI_TXN_3

AC2 DMI_MCH_MT_IR_0_DP C50
AD2 DMI_MCH_MT_IR_0_DN C52
AD4 DMI_MCH_MT_IR_1_DP C51
AE4 DMI_MCH_MT_IR_1_DN C53
AE2 DMI_MCH_MT_IR_2_DP C54
AE2 DMI_MCH_MT_IR_2_DN C57
AF4 DMI_MCH_MT_IR_3_DP C55
AG4 DMI_MCH_MT_IR_3_DN C58

0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_0_DP [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_0_DN [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_1_DP [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_1_DN [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_2_DP [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_2_DN [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_3_DP [18]
0.1u/4/X7R/16V/K >>> DMI_ICH_MT_IR_3_DN [18]

[21] SRCCLK_MCH <> SRCCLK_MCH D9
[21] -SRCCLK_MCH <> -SRCCLK_MCH E9

EXP_CLKP
EXP_CLKN
SDVO_CTRLDATA
SDVO_CTRLCLK

EXP_RCOMP
EXP_COMPI
EXP_ICOMP

Y7
Y8
Y6

GRCOMP
VCC1_1
R93
49.9/4/1

[14] SDVO_CTRL_DATA <> SDVO_CTRL_DATA J13
[14] SDVO_CTRL_CLK <> SDVO_CTRL_CLK G13

PORTB

AB13
AD13

EXP_RBIAS

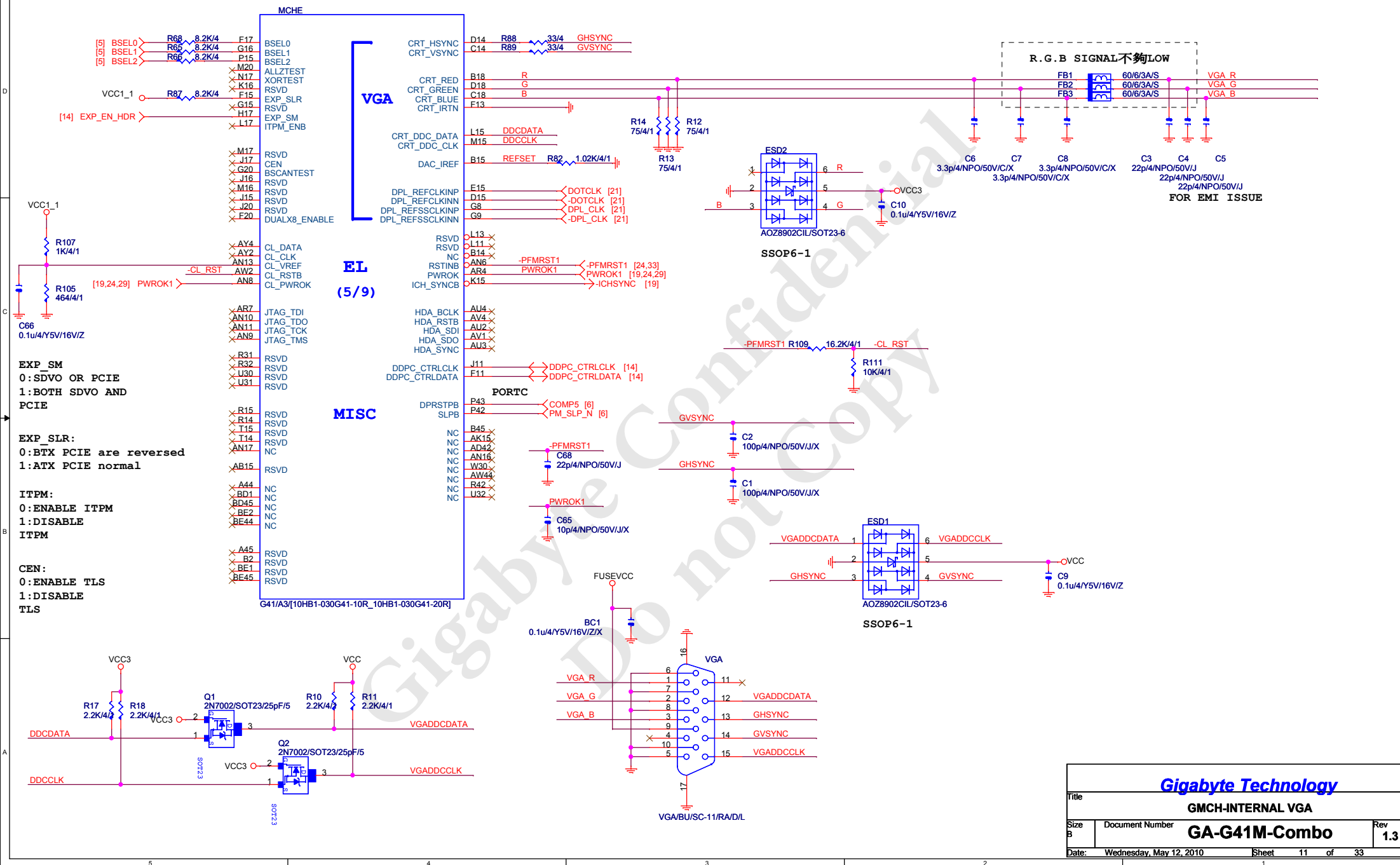
AG1

GRBIAS
R96
750/4/1

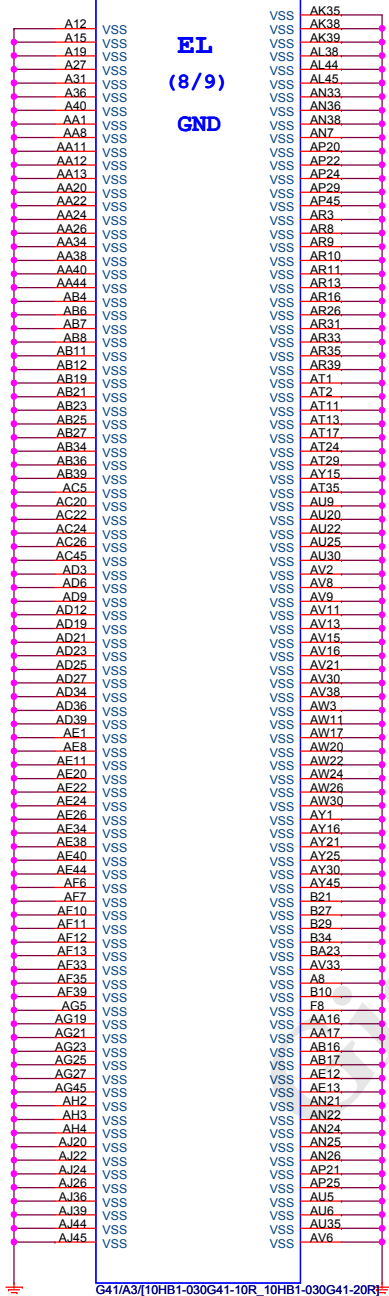
G41/A3/(10HB1-030G41-10R_10HB1-030G41-20R)

Gigabyte Technology

Title			GMCH-PCI E & DMI	
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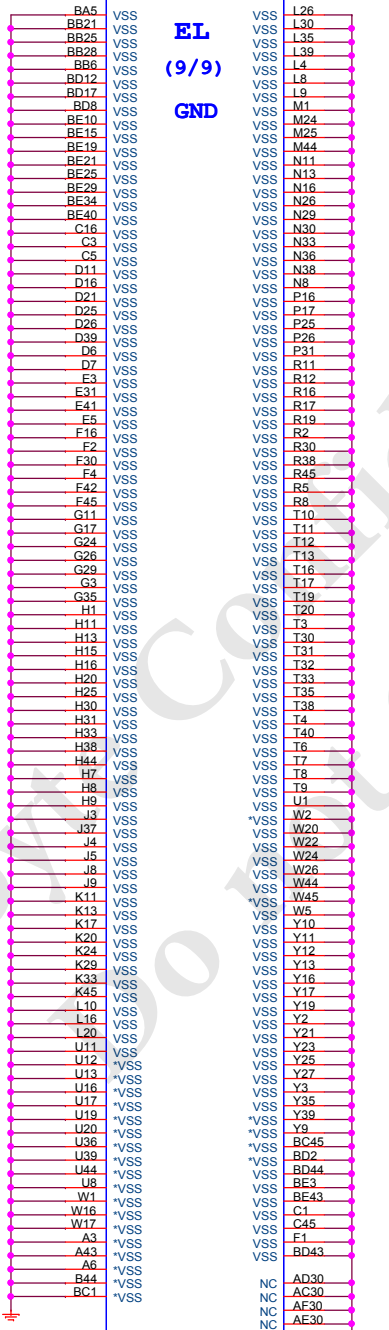


MCHH

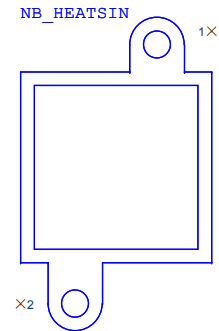


G41/A3/[10HB1-030G41-10R_10HB1-030G41-20R]

MCHI



G41/A3/[10HB1-030G41-10R_10HB1-030G41-20R]

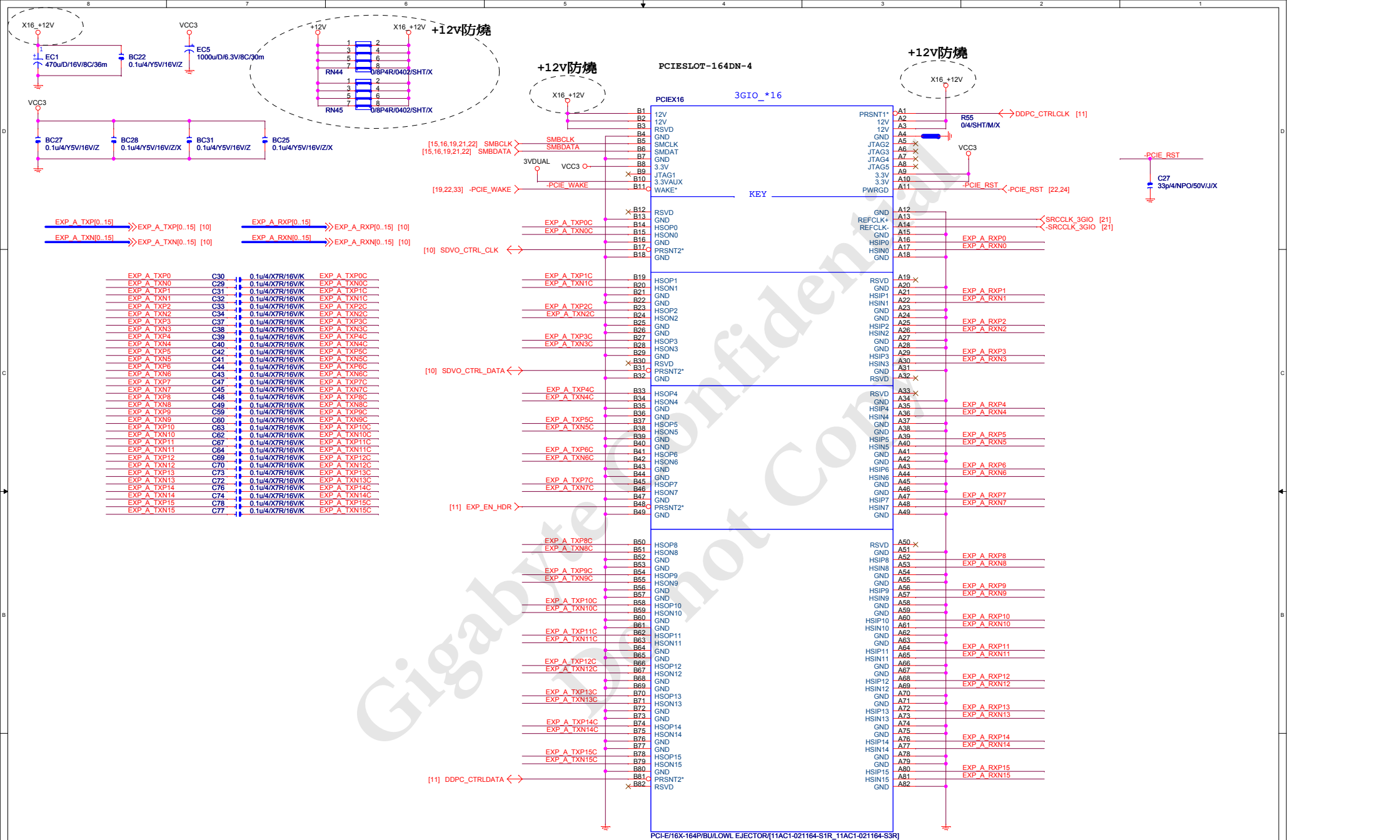


NB_HS

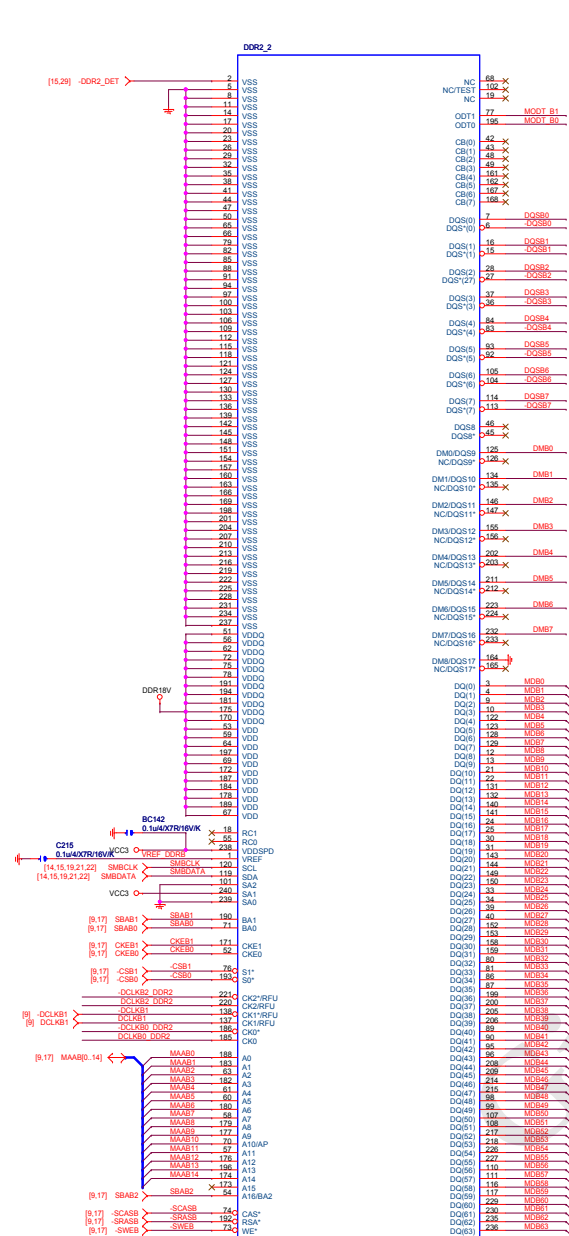
NB_HEATSINK[12SP2-04A004-42R_12SP2-04A004-43R]

BGASINK445A-L GRAY 20MM

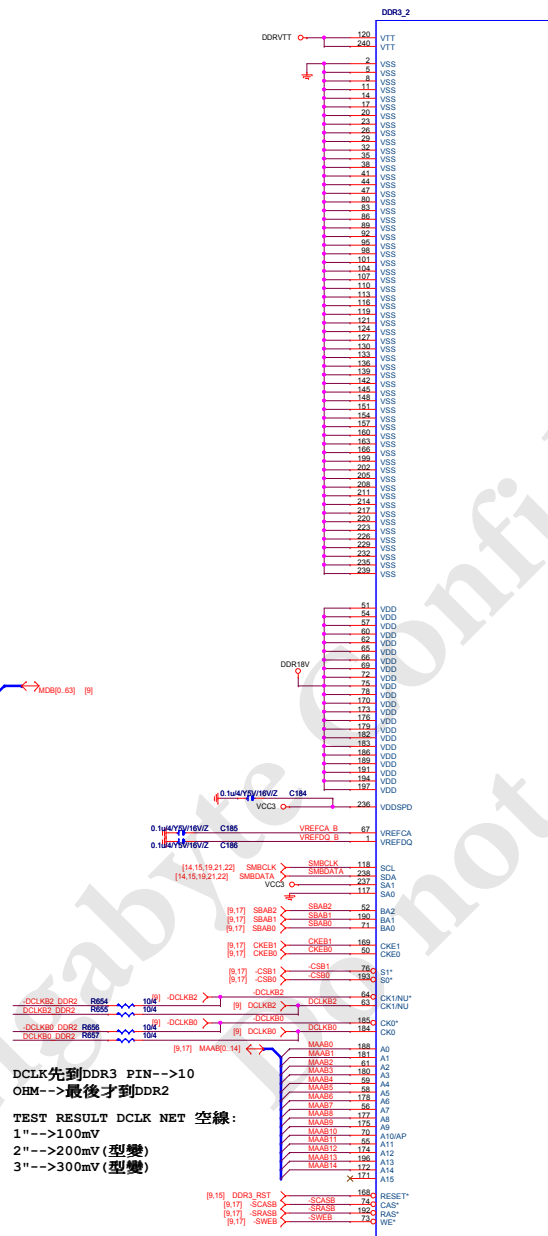
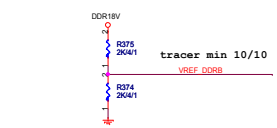
Gigabyte Technology			
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GMCH-GND			
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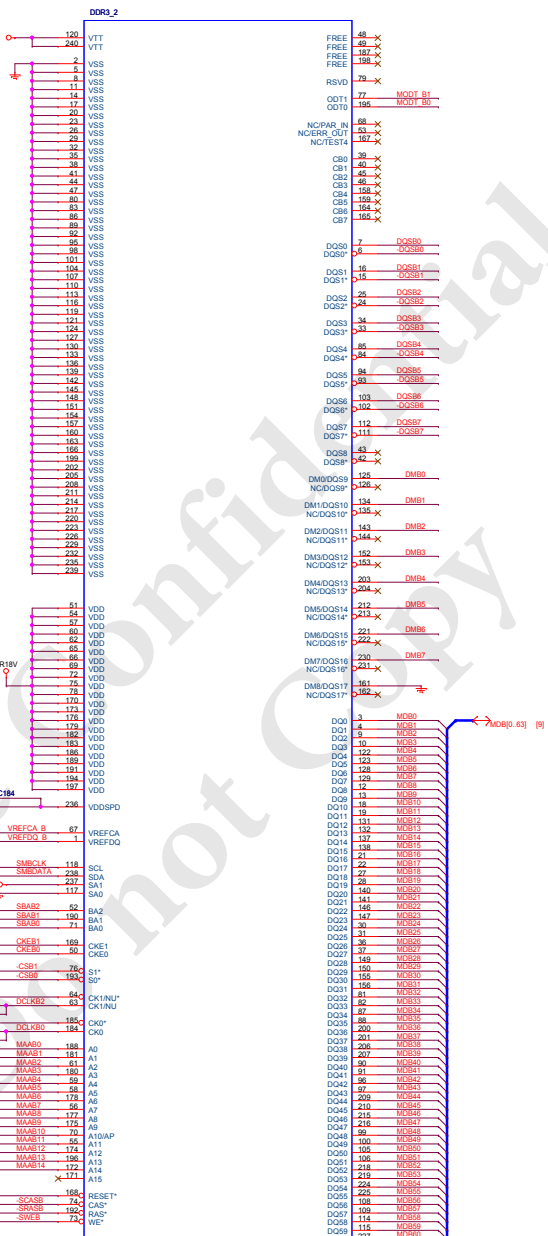
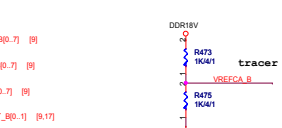
LOWV LEFT BLUE



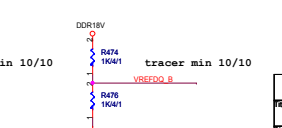
DDR2 SLOT --> WHITE



DDR3 SLOT --> BLUE

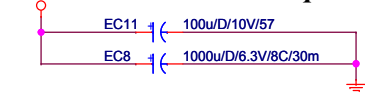


DDR3 SLOT --> BLUE

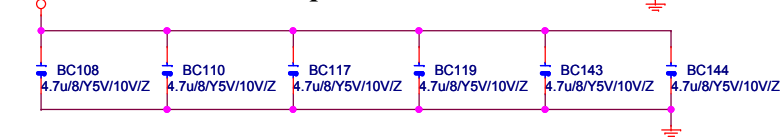


DDR TERMINATION CHANNEL A

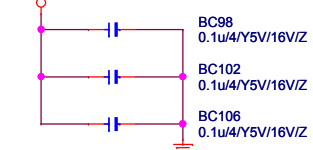
DDR18V Decouple



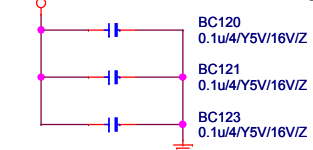
DDRVTT Decouple



DDR18V Decouple



DDRVTT Decouple



SBAA[0..2] < SBAA[0..2] [9,15]

-CSA[0..1] < -CSA[0..1] [9,15]

CKEA[0..1] < CKEA[0..1] [9,15]

MAAA[0..14] < MAAA[0..14] [9,15]

MODT_A[0..1] < MODT_A[0..1] [9,15]

MODT_B[0..1] < MODT_B[0..1] [9,16]

SBAB[0..2] < SBAB[0..2] [9,16]

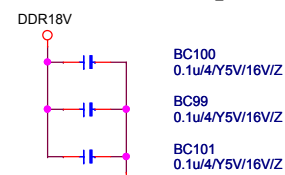
-CSB[0..1] < -CSB[0..1] [9,16]

CKEB[0..1] < CKEB[0..1] [9,16]

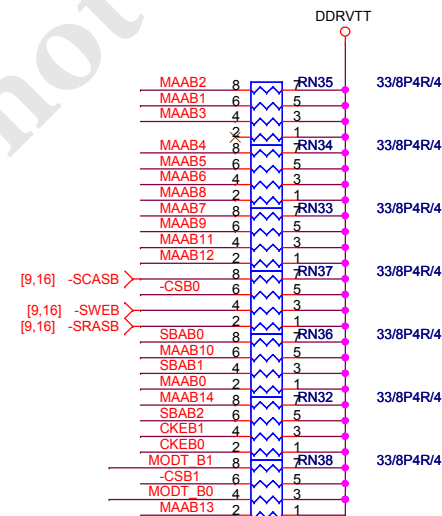
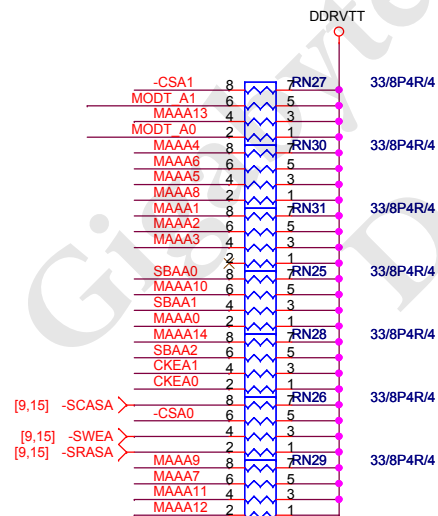
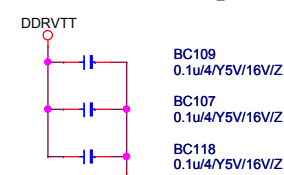
MAAB[0..14] < MAAB[0..14] [9,16]

DDR TERMINATION CHANNEL B

DDR18V Decouple

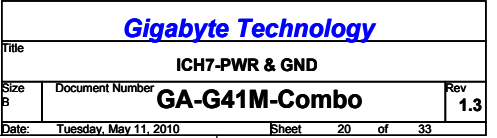


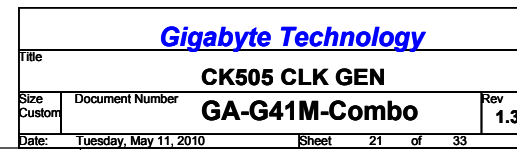
DDRVTT Decouple



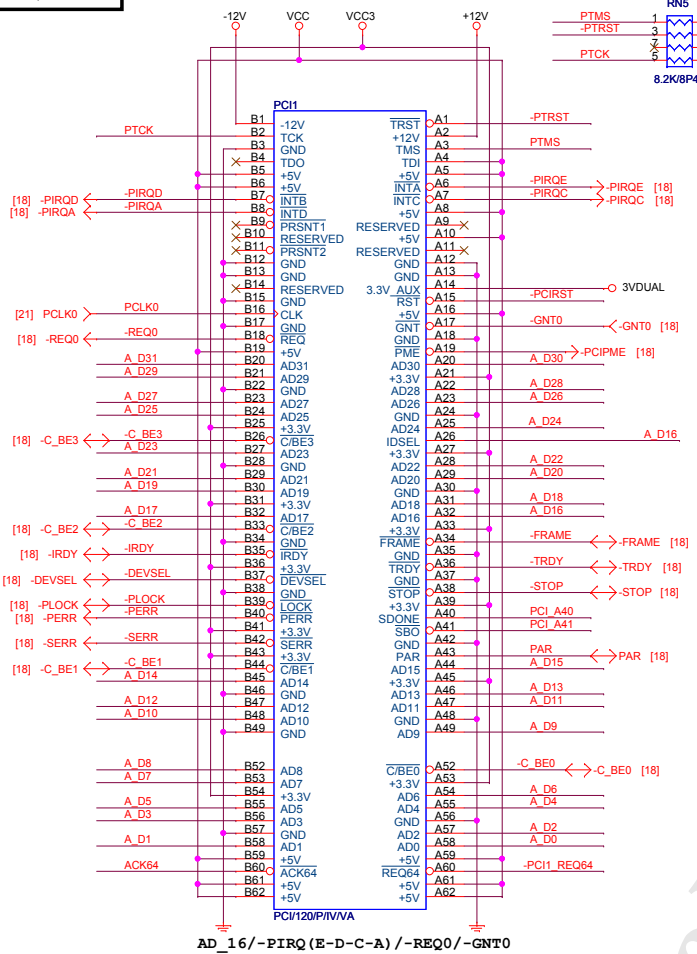
Gigabyte Technology

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DDRII TERMINATOR			
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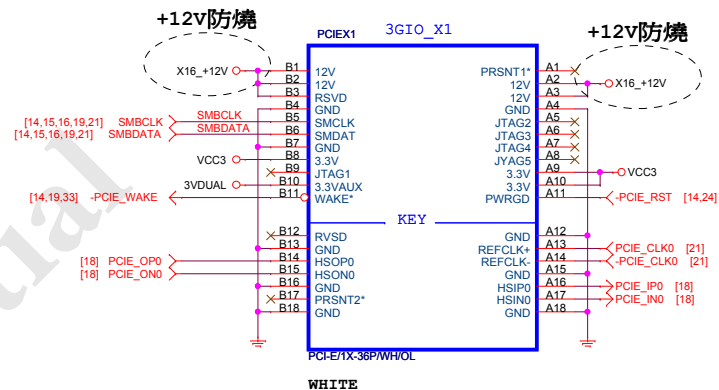
PCI1, 2 SLOT



AD_16/-PIRQ (E-D-C-A) /-REQ0/-GNT0

AD_17/-PIRQ (D-C-A-E) /-REQ1/-GNT1

PCIEX1



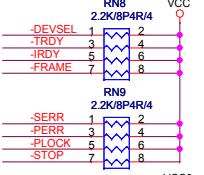
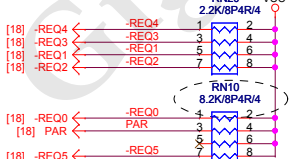
WHITE

[18] A_D[0..31] ↔ A_D[0..31]

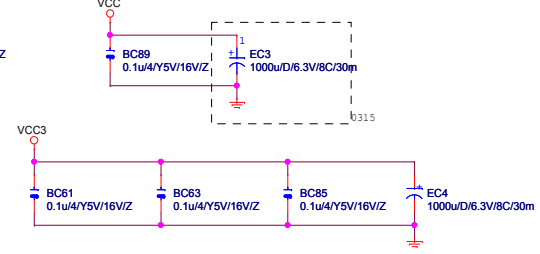
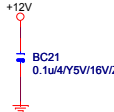
-PCIRST ↔ -PCIRST [18]

Place close to PCI1

[14,15,16,19,21] SMBCLK ↔ PCI_A40
[14,15,16,19,21] SMBDATA ↔ PCI_A41



[18] -PIRQA ↔ -PIRQA
[18] -PIRQD ↔ -PIRQD
[18] -PIRQC ↔ -PIRQC
[18] -PIRQB ↔ -PIRQB



Gigabyte Technology

PCI SLOT 1, 2/PCIEX1

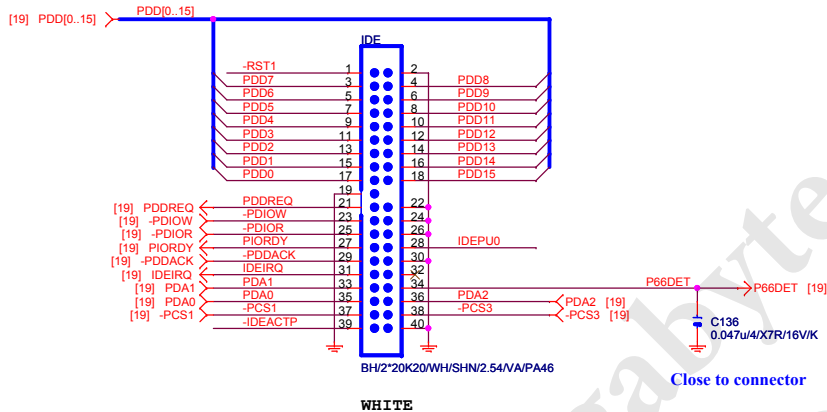
GA-G41M-Combo

Rev 1.3

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The schematic diagram illustrates the LED driver circuit. It features a -SATALED input connected to a resistor R229 (8.2K/4) and a diode D7 (CD4148WP/1208/300mA) in series with a -IDEACTP input. The output of the diode is connected to a node that branches to a resistor R227 (8.2K/4) and a capacitor C149 (180pF/4/NPO/50V/J/X). The node after R227 is connected to the base of a PNP transistor Q28 (MMBT2222A/SOT23/600mA/40). The emitter of Q28 is connected to ground. The collector of Q28 is connected to the base of an NPN transistor Q21 (MMBT2222A/SOT23/600mA/40). The emitter of Q21 is connected to ground. The collector of Q21 is connected to the -HDLED output. The circuit is powered by VCC3.

Pinout diagram for the BH2-17K5/WH/SHN/2.54/A/PA46 connector. The diagram shows a 34-pin connector with pins numbered 1 to 34. Pins 1, 3, 5, 7, 9, 11, 13, 15, 17, 19, 21, 23, 25, 27, 29, 31, and 33 are connected to an FDD. Pins 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are connected to a VCC line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a DENSEL- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to an INDEX- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a MOTEA- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a DRVA- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a DIR- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a STEP- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a WDATA- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a WGATE- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a TK00- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a WPT- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a RDATA- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a SIDE1- signal line. Pins 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30, 32, and 34 are also connected to a DSKCHG- signal line.



The diagram shows the USB1 module with the following connections:

- Signal Connections:**
 - Pin 1:** +USBP0
 - Pin 2:** Ground
 - Pin 3:** +USBP1
 - Pin 4:** -USBP1
 - Pin 5:** Ground
 - Pin 6:** -USBP0
- Protection Network:**
 - A diode network labeled **ESD3** (AOZ8902CIL/SOT23-6) is connected between pins 1, 2, 3, and 4.
 - A fuse labeled **FUSEVCC** is connected between pin 5 and ground.
 - A capacitor labeled **BC92** (0.1uH/Y5V/16V/Z) is connected between pin 6 and ground.

The schematic diagram illustrates the internal wiring of the USB2 module. It features two main components: the F_USB2 chip and the BC96 diode.

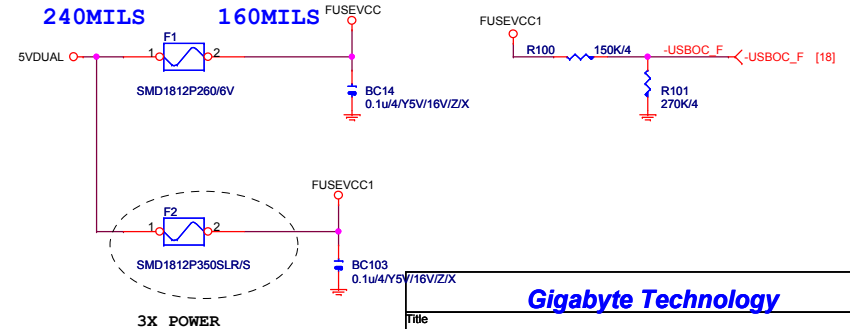
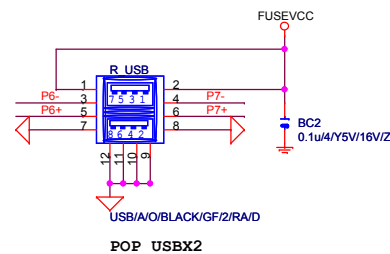
F_USB2 Chip: This chip is a 10-pin component. Its pins are connected as follows:

- Pins 1 and 2 are connected to +USBP2.
- Pins 3 and 4 are connected to +USBP3.
- Pins 5 and 6 are connected to -USBP2.
- Pins 7 and 8 are connected to -USBP3.
- Pins 9 and 10 are connected to FUSEVCC1.

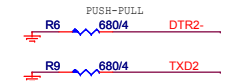
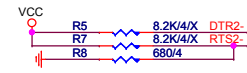
BC96 Diode: This diode is connected in series with the FUSEVCC1 line. Its cathode is connected to the FUSEVCC1 line, and its anode is connected to ground.

Power Connections: The module is powered by +USBP2, +USBP3, -USBP2, and -USBP3. The FUSEVCC1 line is connected to the FUSEVCC1 pin of the F_USB2 chip and the cathode of the BC96 diode.

Grounding: The module is grounded at several points, including the ground pins of the F_USB2 chip and the anode of the BC96 diode.

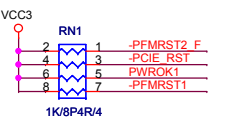
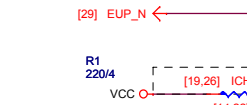


RTS2- ==LOW CPU FAN 50%
==HIGH 100%
DEFAULT 50%



MAC ADDRESS-->N/A ISSUE

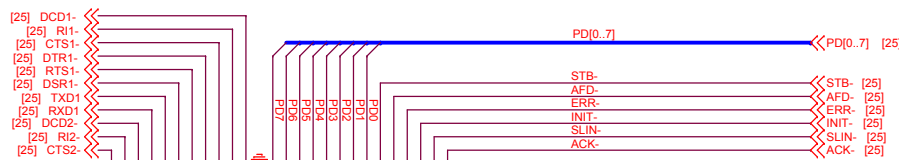
ErP



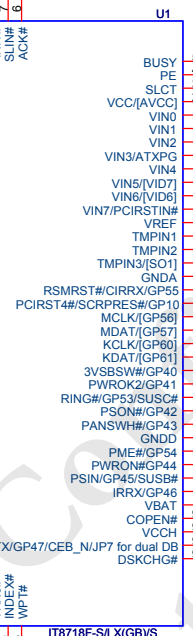
Dual BIOS:
GB logo :Pin 61 (GP15/CSA)
GB logo :Pin 59 (GP17/CSB)

Pin 59 Dual BIOS ,Power On Strapping:
H ==>Dual BIOS function Enable
L ==>Dual BIOS function Disable

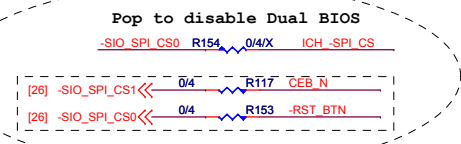
1.2V or 3.3V tolerance select.
1.2V OUTPUT 接 VTT_GMCH
3.3V OUTPUT 接 3.3V
LPCPD# =VIDVCC



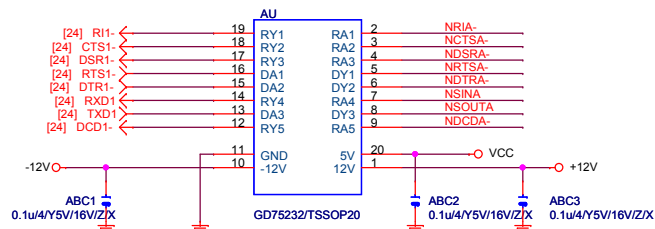
IT8712F/[IT8718F]



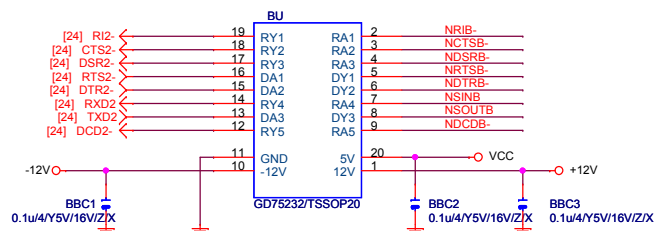
JP7 : HIGH DUAL BIOS ENABLE
LOW DUAL BIOS DISABLE



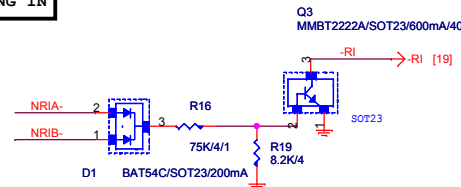
COMA



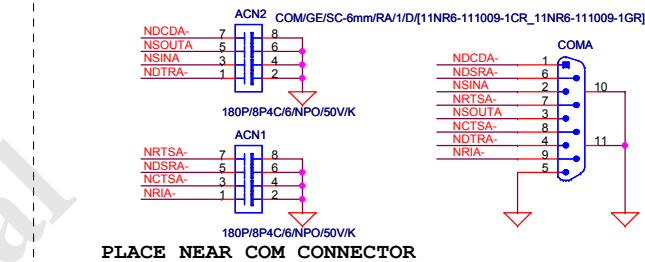
IC20TSSOP-1



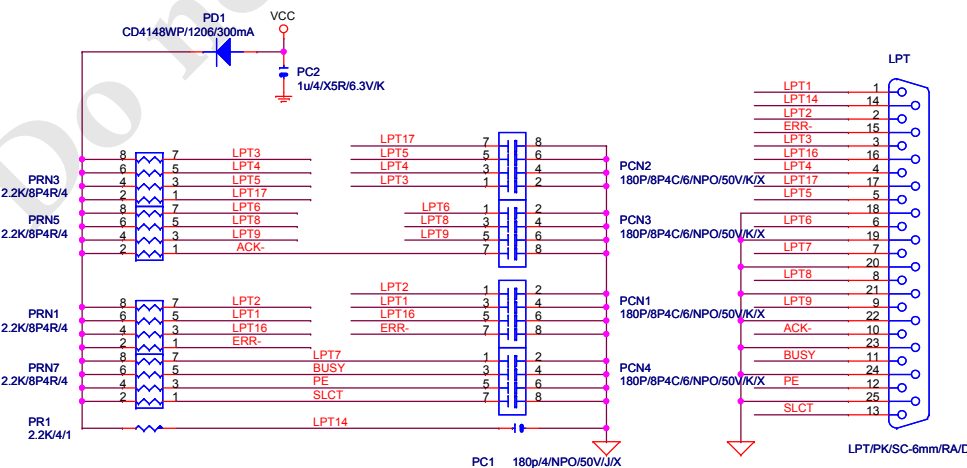
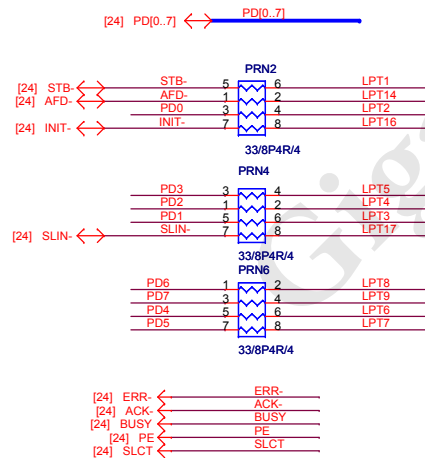
RING IN



EXTERNAL COMA

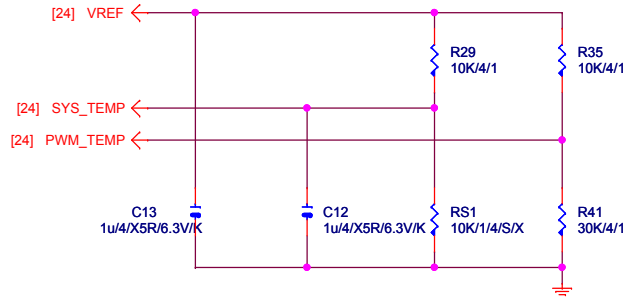


LPT PORT

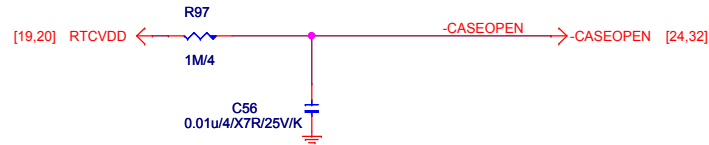


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TEMP H/W MONITOR

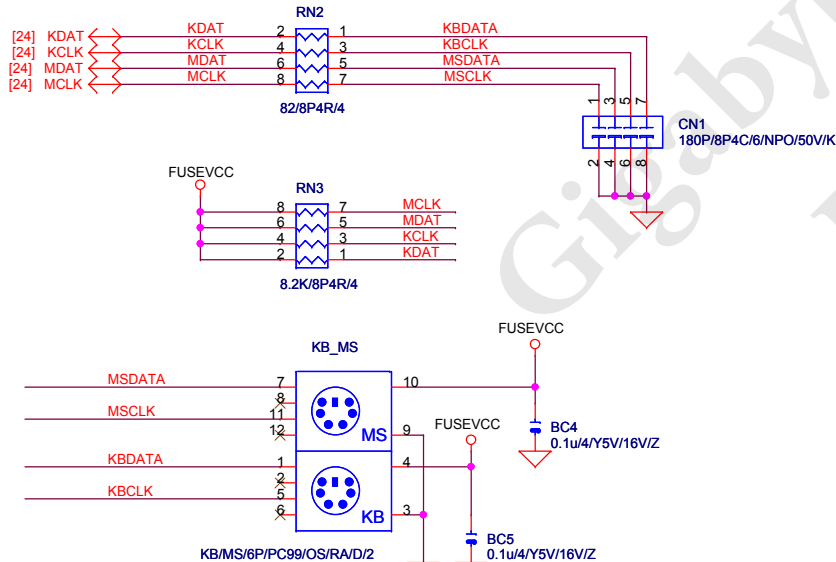


CASE OPEN

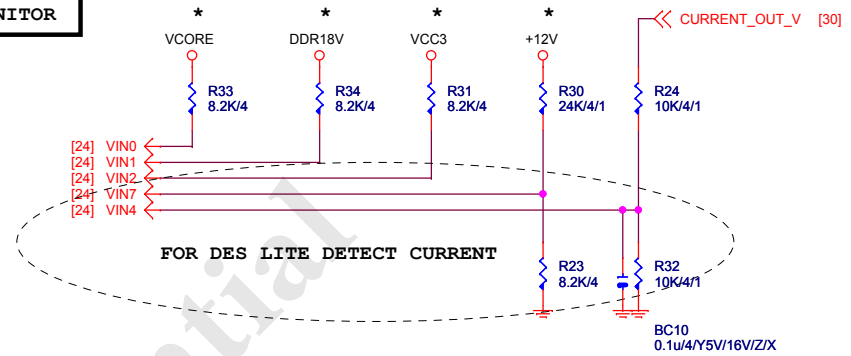


Case Open Circuits

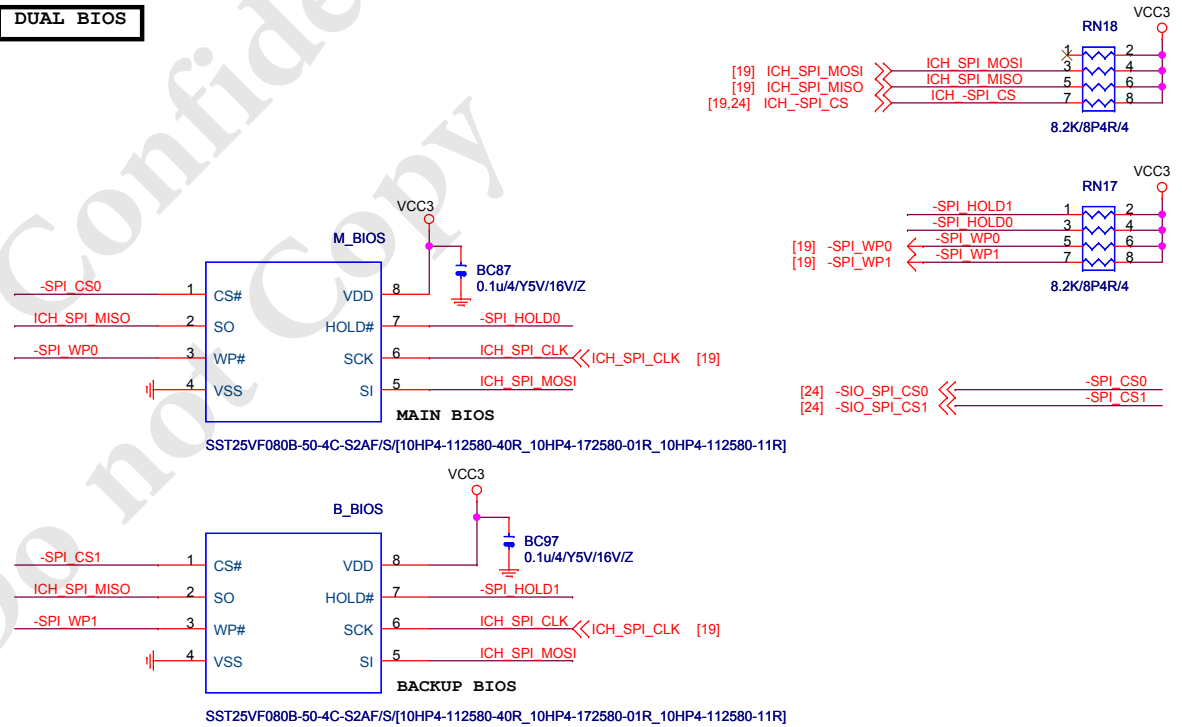
KB/MS



VOLTAGE-- H/W MONITOR



DUAL BIOS

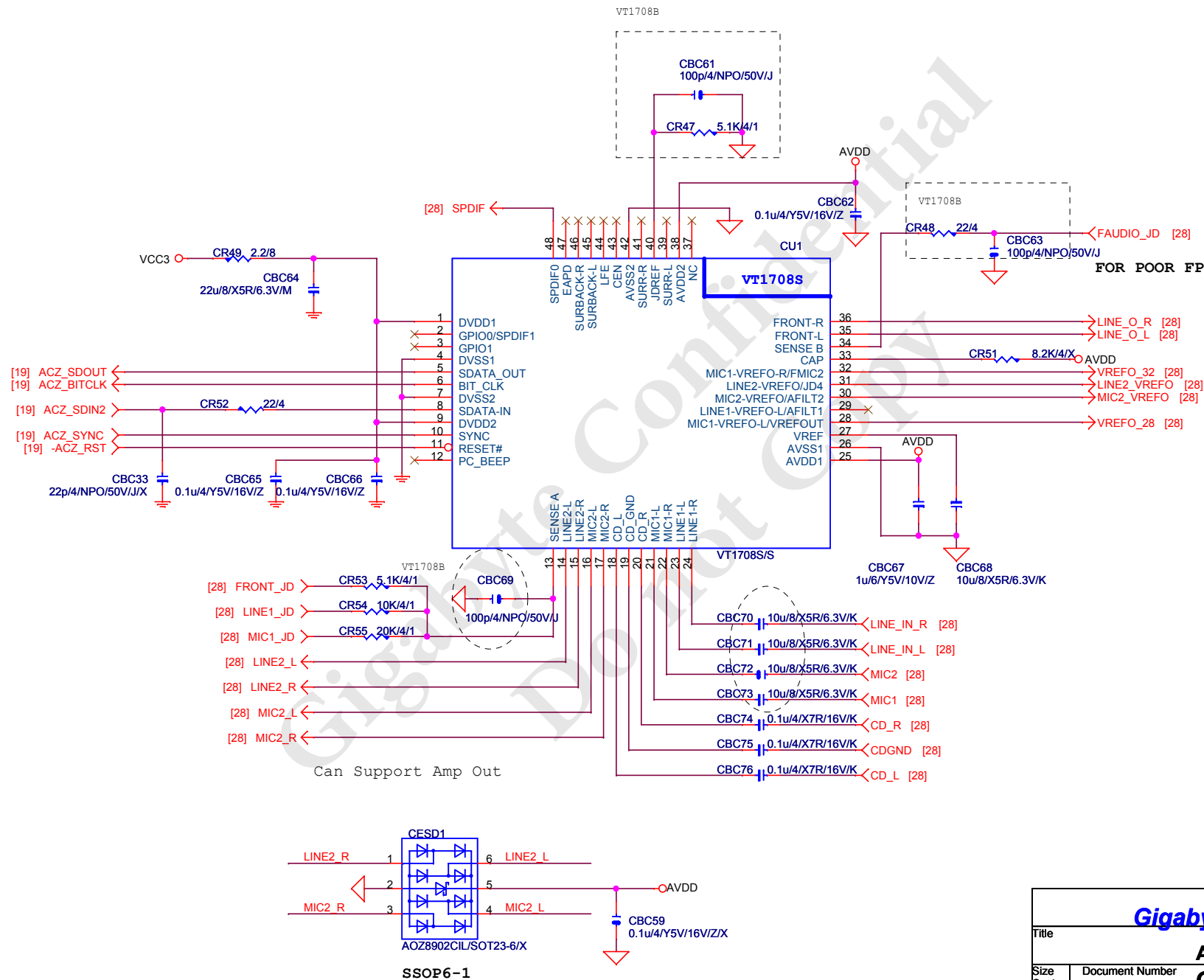


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HW-MONITOR/CI/KB/MS/BIOS

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Custom	GA-G41M-Combo	1.3

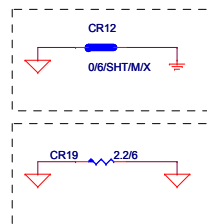
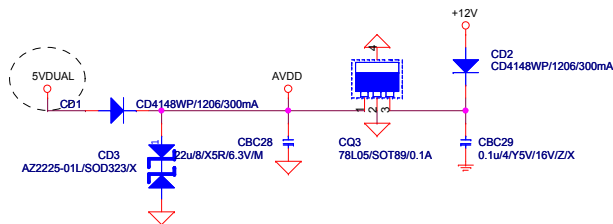
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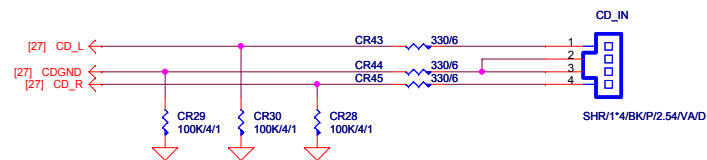
Gigabyte Technology

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Size	Document Number			Rev
Custom	GA-G41M-Combo			1.3
Date:	Wednesday, May 12, 2010	Sheet	27	of 33

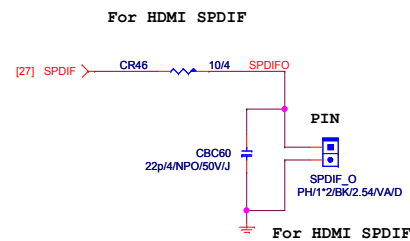
CODEC POWER/EMI PAD



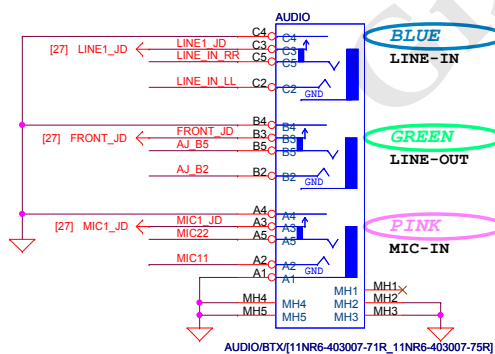
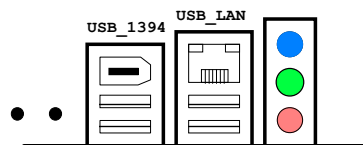
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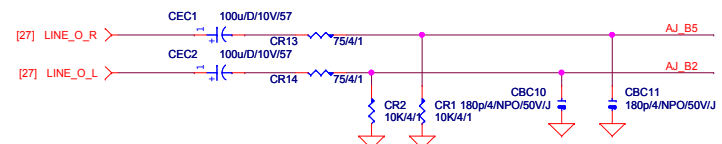
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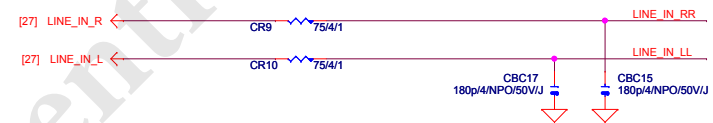
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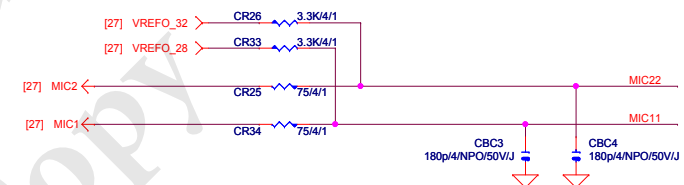
LINE-OUT



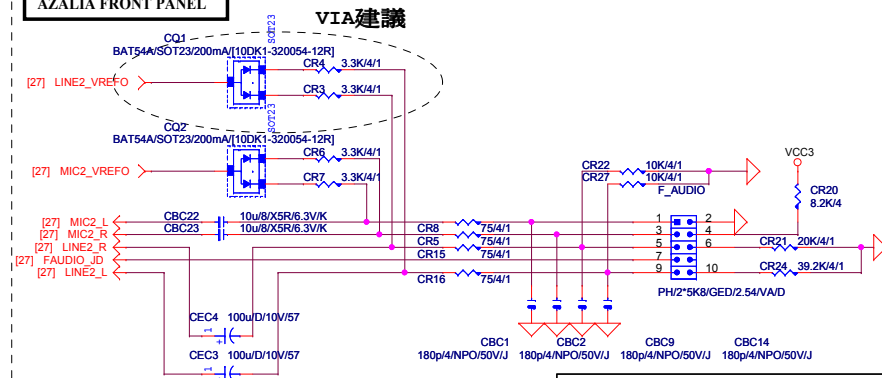
LINE-IN



MIC-IN

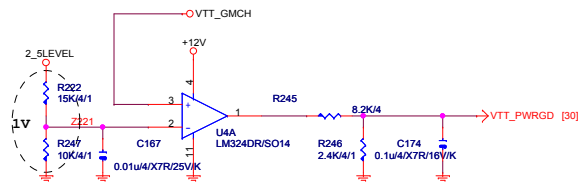


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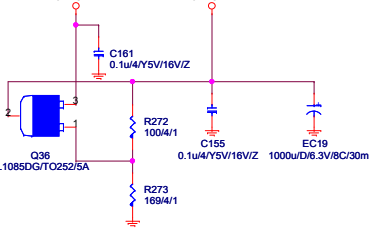


Gigabyte Technology			
Title			
AUDIO JACK			
Size			
Custom			
Document Number			
GA-G41M-Combo			
Rev			
1.3			
Date: Tuesday, May 11, 2010			
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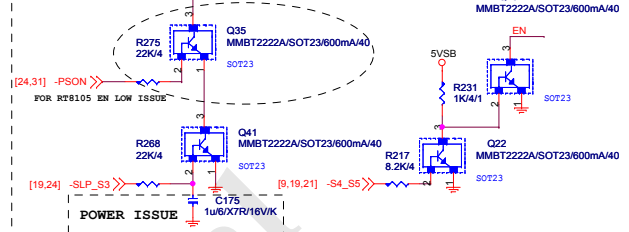
VTT_PWRGD



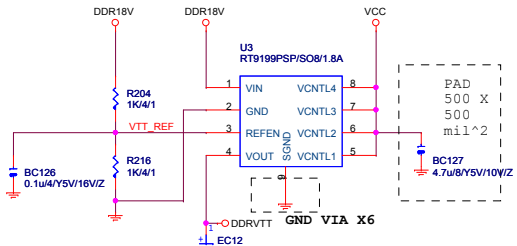
3VDUAL



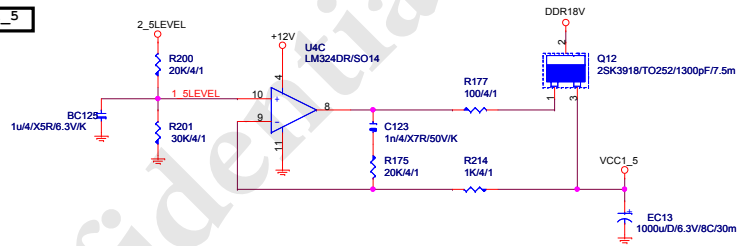
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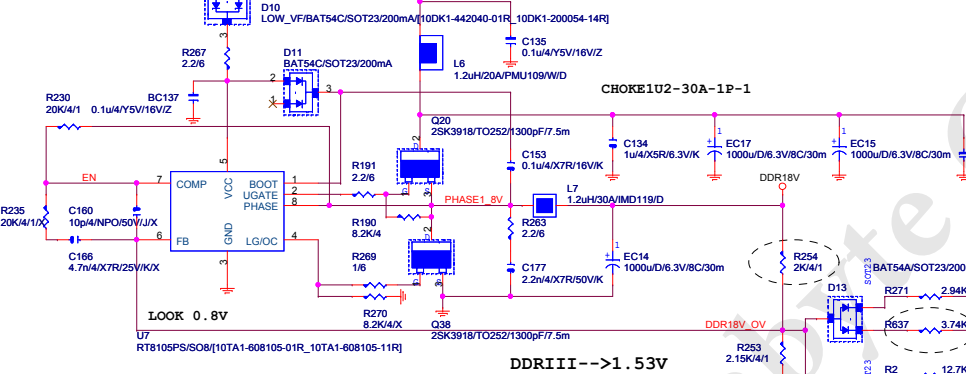
DDR_VTT



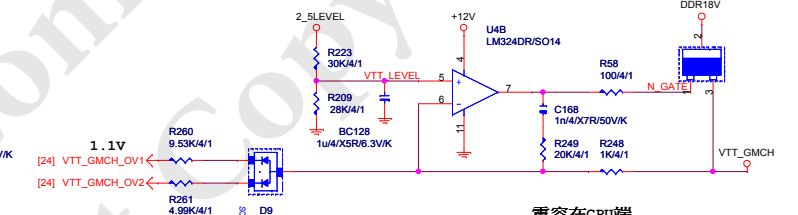
VCC1_5



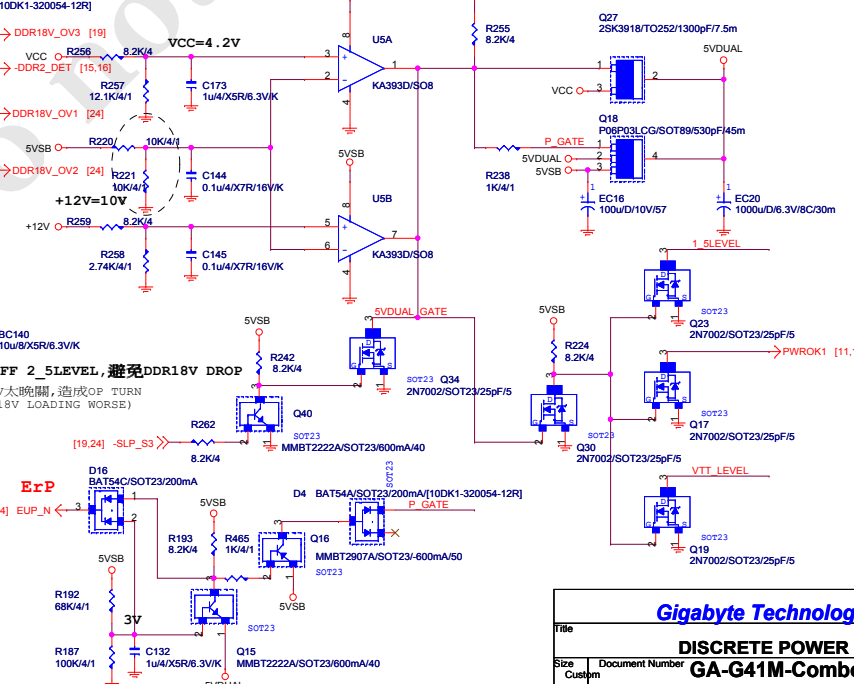
DDR18V



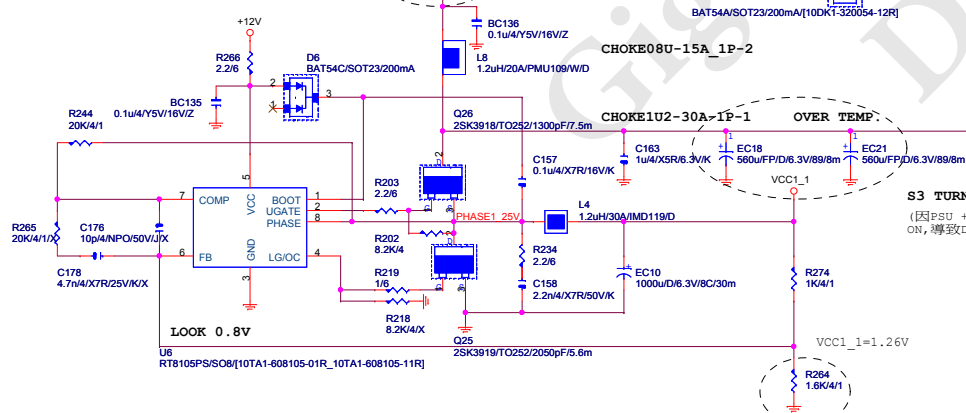
VTT_GMCH

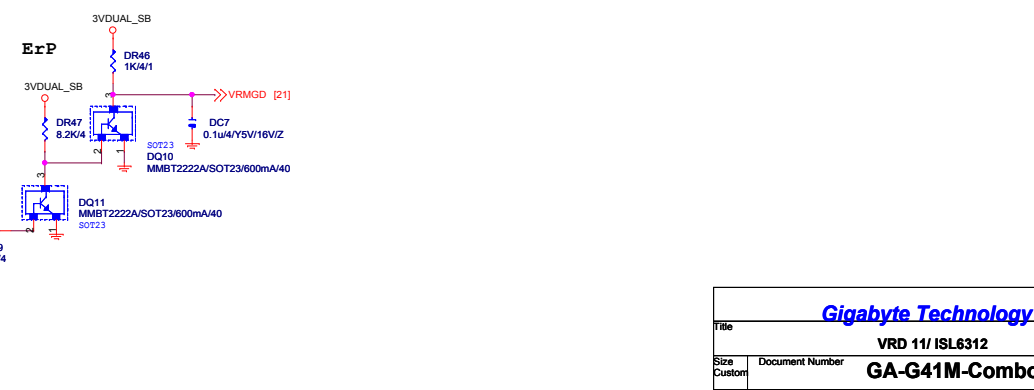
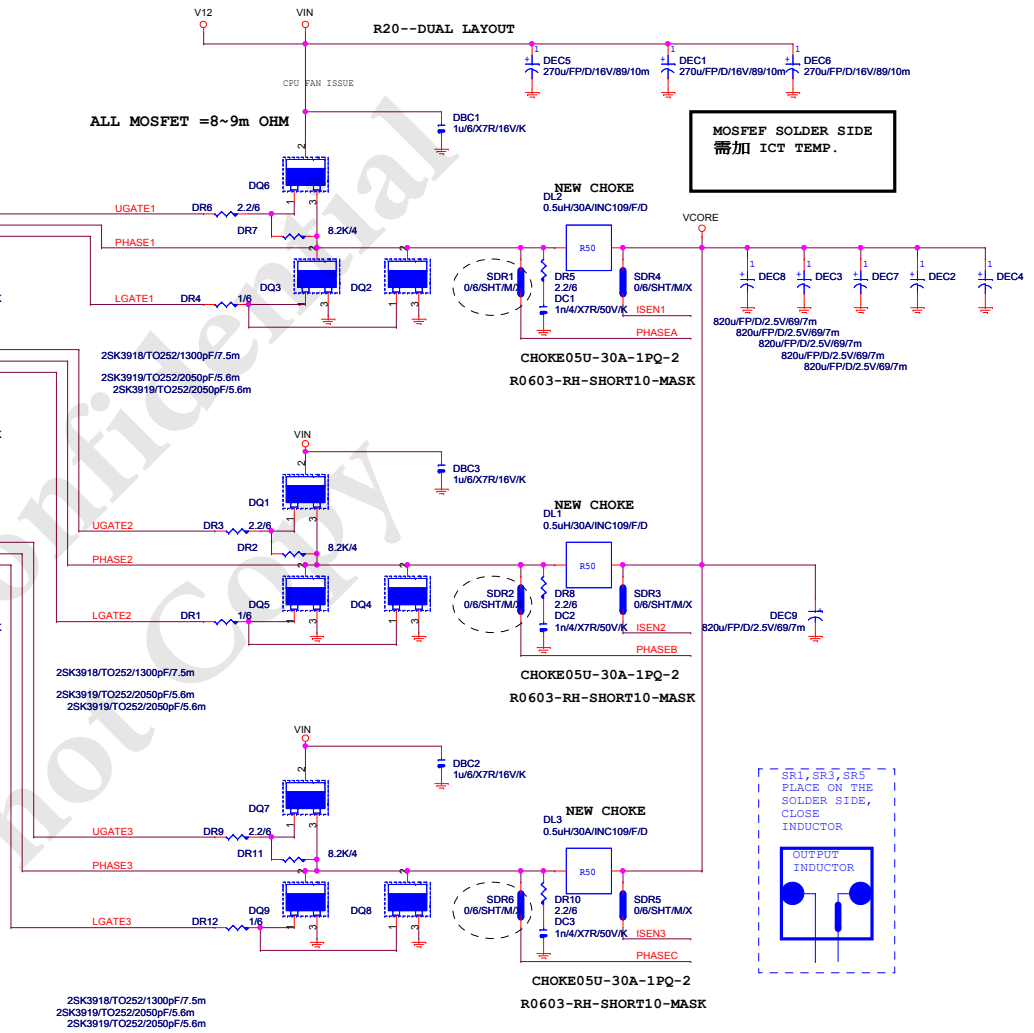
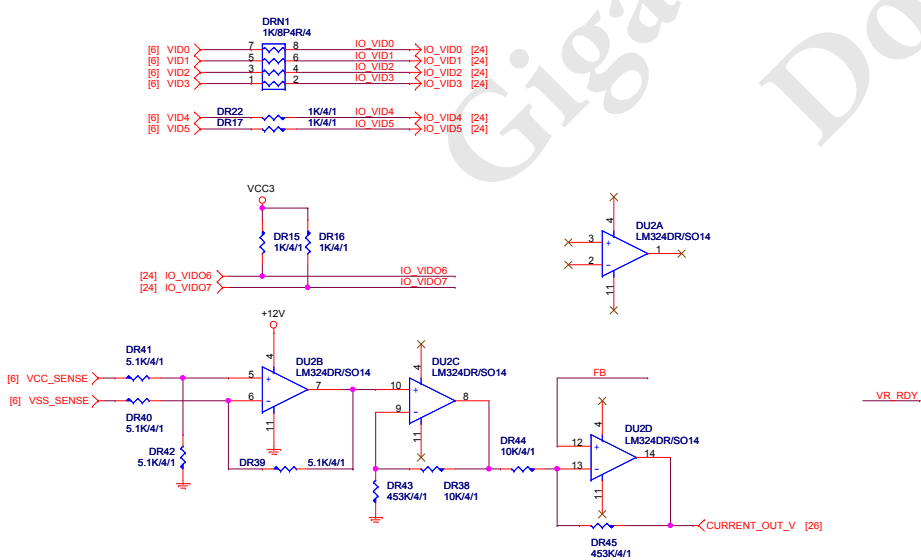
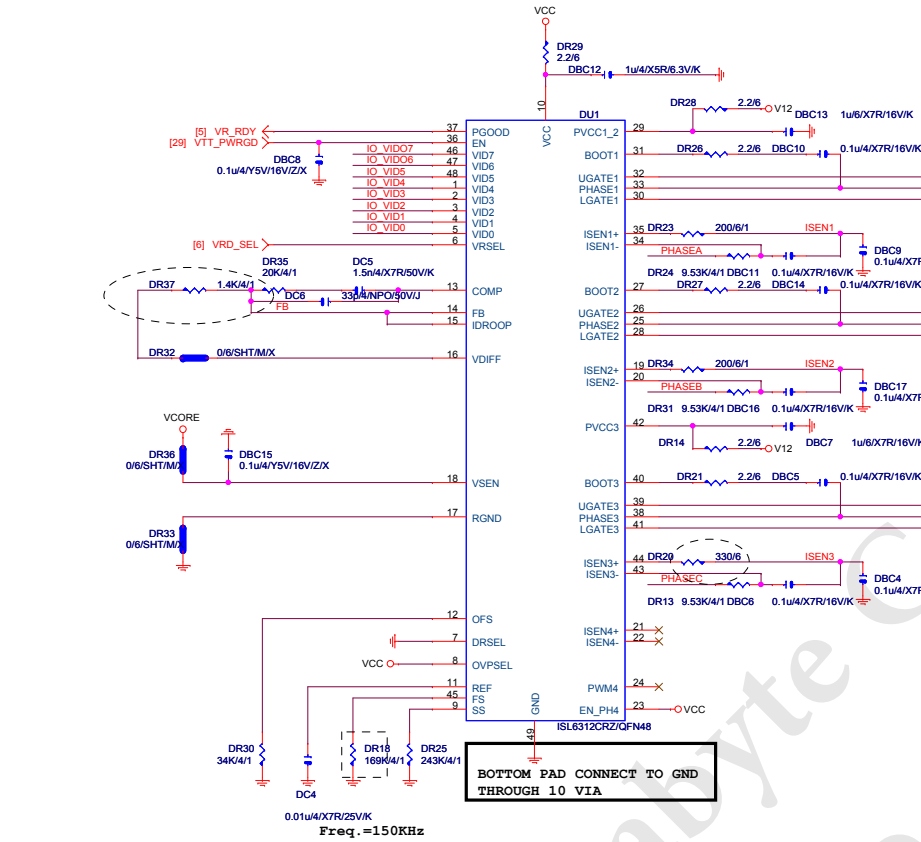


5VDUAL

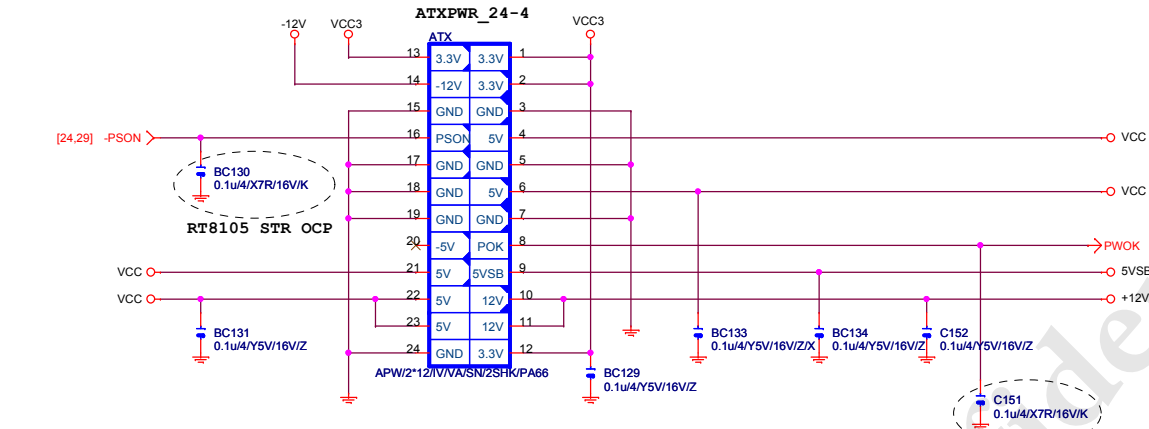


VCC1_1

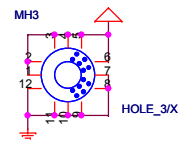
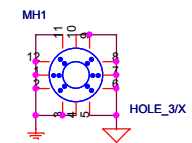
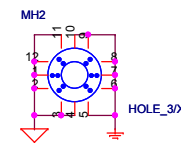
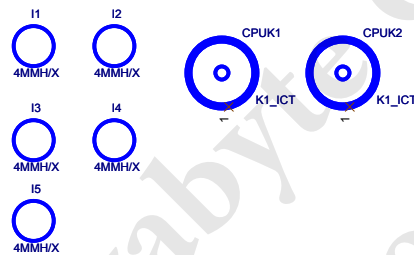
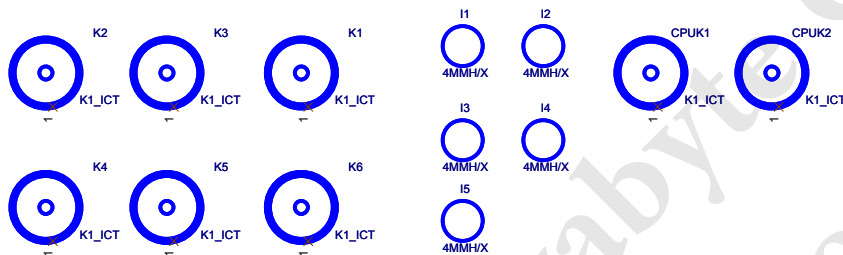
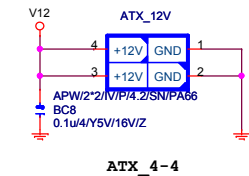
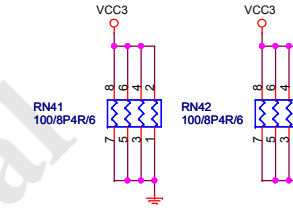




ATX POWER CONNECTOR

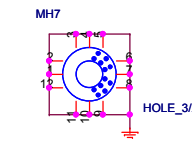
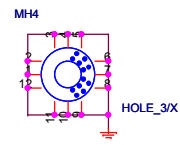
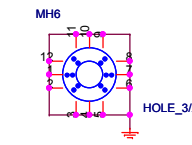
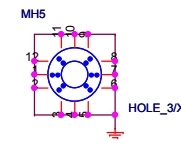


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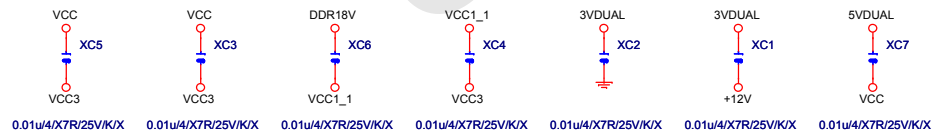


HOLE_4-RH-1

HOLE_4-RH-5MM-1



HOLE_4-RH-5MM-1



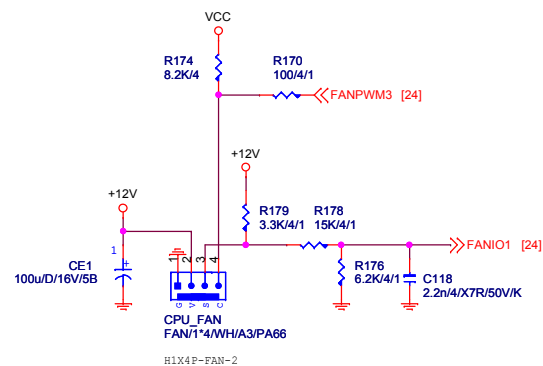
Gigabyte Technology

ATX POWER CONNECTOR

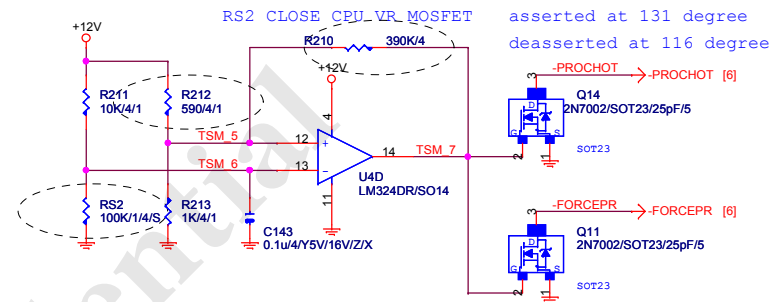
GA-G41M-Combo

Rev 1.3

CPU SMART FAN SMART FAN

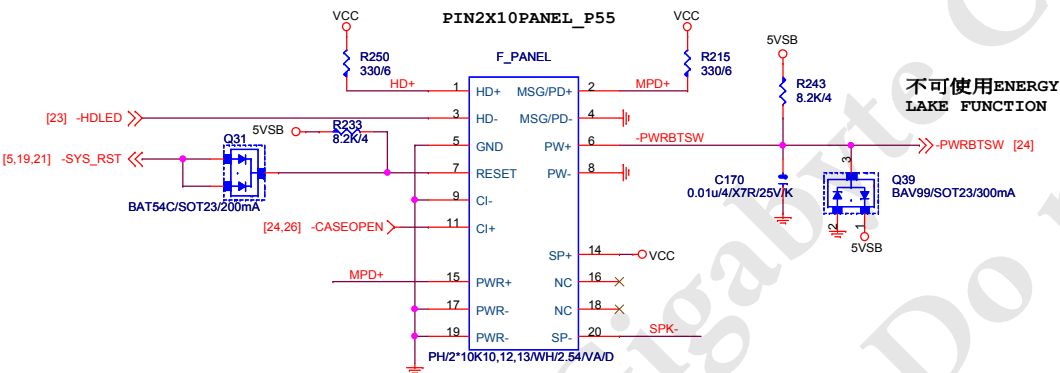


PROCESSOR HOT

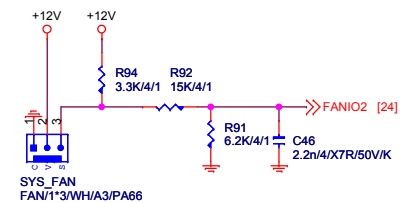


INTEL FRONT PANEL

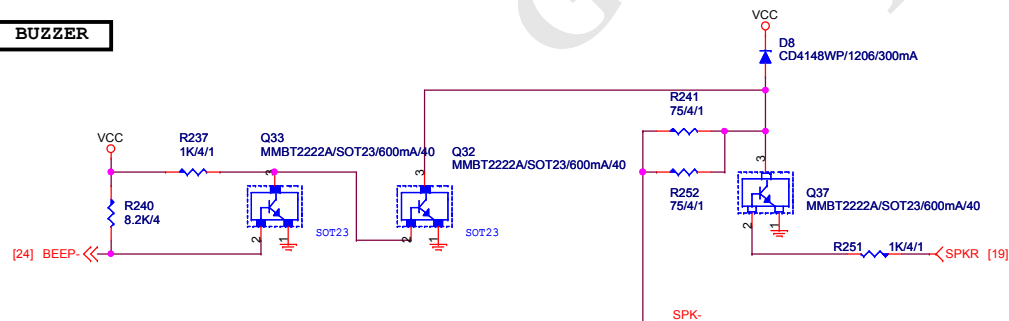
SYS_FAN



不可使用ENERGY LAKE FUNCTION



BUZZER



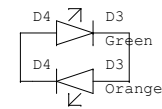
Gigabyte Technology

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Size	Document Number	GA-G41M-Combo	
Custom		Rev	1.3
Date:	Monday, May 10, 2010	Sheet	32 of 33

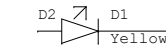
PCIE-1G LAN

CHOK4U7-500MA-1

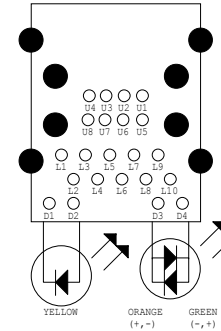
Dual Color LED



Single Color LED



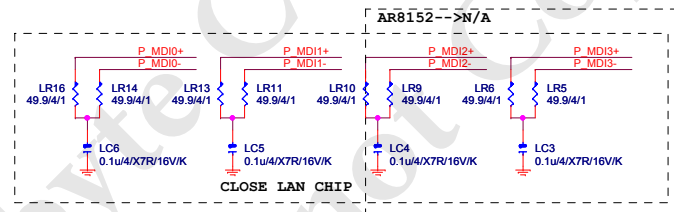
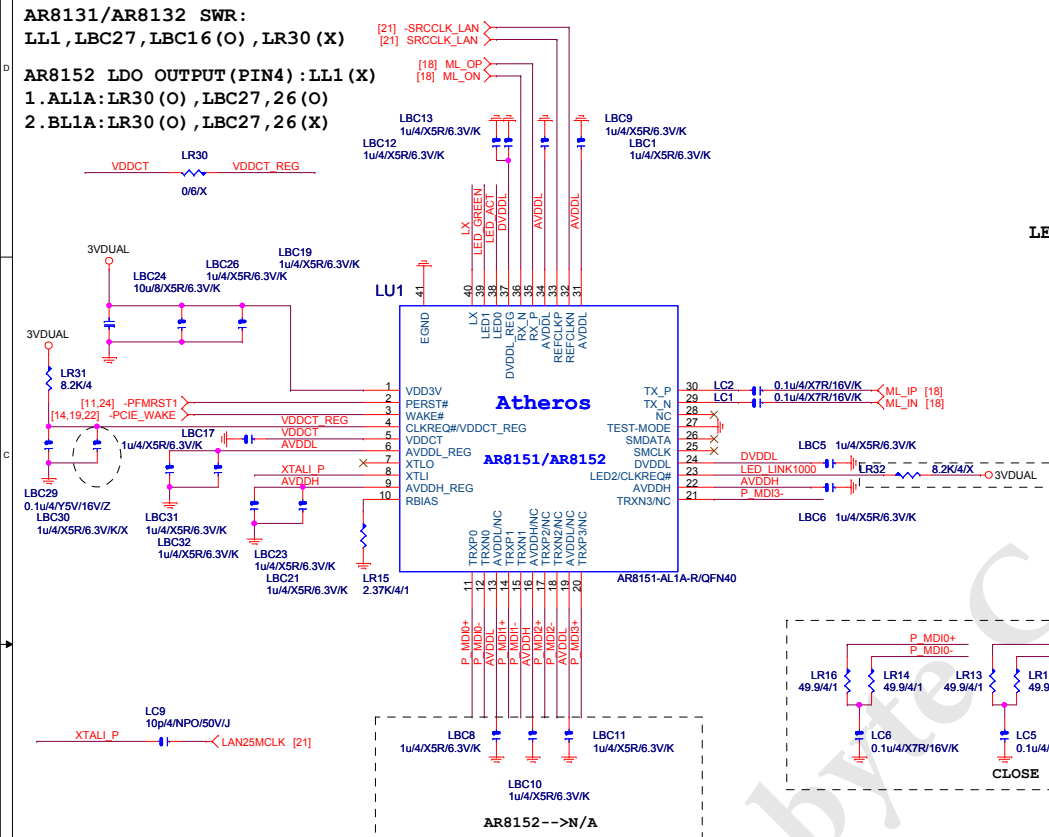
P35-152-19W9



LED0 (ACT) LED1 (LINK) LED2 (LINK1G)

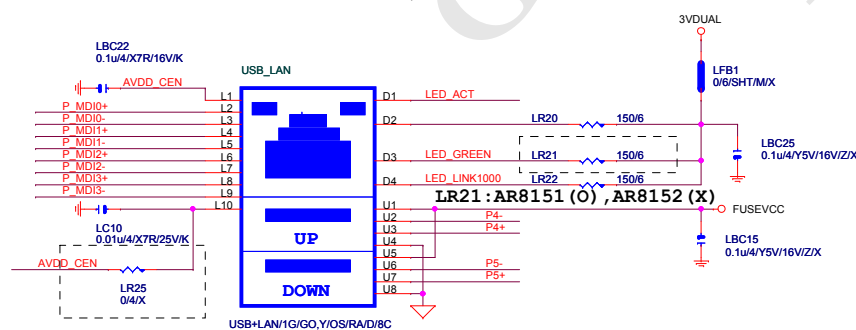
CLKREQ# PULL-UP FOR EFUSE:

- 1.AR8151:LR31 (O) ,LR32 (X)
2.AR8152:LR31 (X) ,LR32 (O)



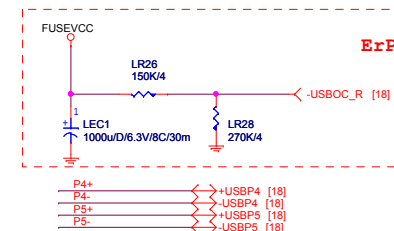
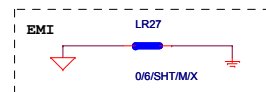
USB_LAN CONNECTOR

```
1G :USB+LAN/1G/GO,Y/OS/RA/D/1
100M:USB+LAN/100/GO,Y/OS/RA/D/1
```



LR25:AR8151 (X) ,AR8152 (O)
 因100M LAN CONNECTOR差異

USB LAN



Gigabyte Technology

ATHEROS AR8151M/AR8152M**GA-G41M-Combo**

Title				Gigabyte Technology			
ATHEROS AR8151M/AR8152M							
Size		Document Number		GA-G41M-Combo		Rev	
Custom						1.3	
Date:		Wednesday, May 12, 2010		Sheet		33 of 33	